

VIDYA JYOTHI INSTITUTE OF TECHNOLOGY, AUTONOMOUS
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE FOR M.TECH (VLSI System Design)(R19)

I Semester

S.No	Category	Course Title	Int. marks	Ext. marks	L	T	P	C
1.	19D4CS1101	VLSI Technology	30	70	4	0	0	4
2.	19D4CS1102	CMOS Analog Integrated Circuit Design	30	70	4	0	0	4
3.	19D4CS1103	CMOS Digital Integrated Circuit Design	30	70	4	0	0	4
4.	19D4E11101 19D4E11102 19D4E11103	Advanced Digital System Design Hardware Software Co-Design Device Modeling	30	70	3	0	0	3
5.	19D4E21101 19D4E21102 19D4E21103	Embedded System Design Advanced Computer Architecture Digital Signal Processors & Architectures	30	70	3	0	0	3
6.	191EOE1101	Internet of Things	30	70	3	0	0	3
7.	19D4LB1101	Digital IC Design Lab	30	70	0	0	3	2
8.	19D4SM1101	Seminar	100	0	0	0	3	2
Total			310	490	21	0	6	25

II Semester

S. No	Category	Course Title	Int. marks	Ext. marks	L	T	P	C
1.	19D4CS1201	CMOS Mixed Signal Circuit Design	30	70	4	0	0	4
2.	19D4CS1202	Low Power VLSI Design	30	70	4	0	0	4
3.	19D4CS1203	Design for Testability	30	70	4	0	0	4
4.	19D4E31201 19D4E31202 19D4E31203	CAD for VLSI Circuits Scripting Languages VLSI Signal Processing	30	70	3	0	0	3
5.	19D4E41201 19D4E41202 19D4E41203	Full custom IC Design System On Chip Architecture Semiconductor Memory Design & Testing	30	70	3	0	0	3
6.	191EOE1201	Artificial Intelligence & Machine Learning	30	70	3	0	0	3
7.	19D4LB1201	Analog IC Design Lab	30	70	0	0	3	2
8.	19D4SM1201	Seminar	100	0	0	0	3	2
Total			310	490	21	0	6	25

III Semester

		Course Title	Int. marks	Ext. marks	L	T	P	C
1.	19DDCS1207	Technical Paper Writing	100	0	0	3	0	2
2.	19D4CV2102	Comprehensive Viva-Voce	0	100	0	0	0	4
3.	19D4PW2101	Project work Review II	100	0	0	0	22	8
		Total	200	100	0	3	22	14

IV Semester

		Course Title	Int. marks	Ext. marks	L	T	P	C
1.	19D4PW2202	Project work Review III	100	0	0	0	24	8
2.	19D4PW2201	Project Evaluation (Viva-Voce)	0	100	0	0	0	16
		Total	100	100	0	0	24	24

***Open Elective subjects must be chosen from the list of open electives offered by OTHER departments.**



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(Aziz Nagar, C.B.Post, Hyderabad -500075)

M.Tech R15 Regulations

M.Tech - VLSI DESIGN (Course Structure)

I Year – I Semester

Subject Code	Category	Course Title	Int. marks	Ext. marks	L	P	C
15D4CS1104	Core Course I	VLSI Technology	40	60	4	--	4
15D4CS1105	Core Course II	CMOS Analog Integrated Circuit Design	40	60	4	--	4
15D4E21106	Core Course III	CMOS Digital Integrated Circuit Design	40	60	4	--	4
15D4E21101 15D4E11101 15D4E21103	Core Elective I	Digital System Design Hardware Software Co-Design CPLD and FPGA Architectures and Applications	40	60	4	--	4
15D4E21104 15D4CS1101 15D4E21105	Core Elective II	Algorithms for VLSI Design Automation Embedded System Design Device Modeling	40	60	4	--	4
15D4OE1103 15D4OE1104 15D4OE1105	Open Elective I	Soft Computing Techniques Image and Video processing Software Defined Radio	40	60	4	--	4
15D4LB1101	Laboratory I	VLSI Laboratory – I	40	60	--	4	2
15D4SM1101	Seminar I	Seminar	50	--	--	4	2
Total Credits					24	8	28

I Year – II Semester

Subject Code	Category	Course Title	Int. marks	Ext. marks	L	P	C
15D4CS1207	Core Course IV	Low Power VLSI Design	40	60	4	--	4
15D4CS1208	Core Course V	Design for Testability	40	60	4	--	4
15D4CS1209	Core Course VI	CMOS Mixed Signal Circuit Design	40	60	4	--	4
15D4E31204 15D4E31205 15D4E31206	Core Elective III	VLSI and DSP Architectures Full custom IC Design Hardware Description Language	40	60	4	--	4
15D4E41204 15D4E41203 15D4E41206	Core Elective IV	Optimization Techniques in VLSI Design System On Chip Architecture Semiconductor Memory Design and Testing	40	60	4	--	4
15D4OE1201 15D4OE1204 15D4OE1202	Open Elective II	Scripting Languages Coding Theory and Techniques Adhoc Wireless Networks	40	60	4	--	4
15D4LB1202	Laboratory II	VLSI Laboratory – II	40	60	--	4	2
15D4SM1202	Seminar II	Seminar	50	--	--	4	2
Total Credits					24	8	28

II Year - I Semester

Subject Code	Course Title	Int. marks	Ext. marks	L	P	C
15D4CV2102	Comprehensive Viva-Voce	--	100	--	--	4
15D4PW2101	Project work Review I	50	--	--	24	12
Total Credits				--	24	16

II Year - II Semester

Subject	Course Title	Int.	Ext.	L	P	C
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M.Tech R15 Regulations

Code		marks	marks			
15D4PW2202	Project work Review II	50	--	--	8	4
15D4PE2201	Project Evaluation (Viva-Voce)	--	150	--	16	12
	Total Credits			--	24	16



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

(Established by an Act No.30 of 2008 of A.P. State Legislature)

Kukatpally, Hyderabad – 500 085, Andhra Pradesh (India)

M.Tech. (VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN)

COURSE STRUCTURE AND SYLLABUS

I Year - I Semester

Code	Group	Subject	L	P	Credits
		VLSI Technology and Design	3	0	3
		CMOS Analog Integrated Circuit Design	3	0	3
		CPLD and FPGA Architectures and Applications	3	0	3
		CMOS Digital Integrated Circuit Design	3	0	3
	Elective -I	Digital System Design	3	0	3
		Hardware Software Co-Design			
		Device Modeling			
	Elective -II	Advance Operating Systems	3	0	3
		Micro Controllers for Embedded System Design			
		Advanced Computer Architecture			
	Lab	VLSI Laboratory – I	0	3	2
		Soft Skills Lab	-	-	2
		Total Credits	18	3	22

I Year - II Semester

Code	Group	Subject	L	P	Credits
		Low Power VLSI Design	3	0	3
		CAD for VLSI Circuits	3	0	3
		CMOS Mixed Signal Circuit Design	3	0	3
		Design for Testability	3	0	3
	Elective - III	Scripting Languages	3	0	3
		Digital Signal Processors and Architectures			
		VLSI Signal Processing			
	Elective – IV	Optimization Techniques in VLSI Design	3	0	3
		System On Chip Architecture			
		Semiconductor Memory Design and Testing			
	Lab	VLSI Laboratory – II	0	3	2
		Seminar	-	-	2
		Total Credits	18	3	22

II Year - I Semester

Code	Group	Subject	L	P	Credits
		Comprehensive Viva	-	-	2
		Project Seminar	0	3	2
		Project work	-	-	18
		Total Credits	-	3	22

II Year - II Semester

Code	Group	Subject	L	P	Credits
		Project work and Seminar	-	-	22
		Total Credits	-	-	22