VIDYA JYOTHI
Institute of Technology
AN AUTONOMOUS INSTITUTION

ANURAG UNIVERSITY

IEEE VJIT Student Branch

Webinar on

Designing of Ternary Logic Gates using Futuristic Nano Devices

20th June 2020

11:00AM to 1:00PM

Dr. V. Ramesh Kumar

Associate Professor
Department of ECE,
Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal

Registration link:
https://forms.gle/7dkW3PUCrMz3nPzd7

IEEE Student Branch Counselor

Dr. M Girish Kumar,
Associate Professor, ECE Dept.,
VJIT, Hyderabad