Vidya Jyothi Institute of Technology

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Innovative Teaching Methods 2020-21

Title of Innovative method/activity : Activity based Learning

Name of the faculty : Dr. C. N. Ravi

Designation : Professor

Course Name **:** Microprocessor and Interfacing Devices

Objectives of method: This activity orients the students such that they are assisted to remember and recall the basic concepts of the course during their examinations. Also inculcate the interest and involvement of students completely during the lecture sessions.

Topic Covered through activity: Memory Organization in the 8086 Microprocessor

Description of method: Two students are assigned BHE and A0, Twenty students are assigned as the address bus and used to locate the address of the data. The multiplexed address data bus – students carry the data back to the microprocessor.

There are 20 address lines in the 8086 microprocessor. This gives us 220 different memory locations. Hence the total size is 220 Bytes (as each memory location is Byte Addressable, i.e. one byte of data can be stored at every single location), which is equal to 1MB. Even the memory is byte-addressable, yet the 8086 microprocessor an easily handle up to 16 bits of data at a time through its 16 data lines. So, to organize the memory efficiently, the entire memory in 8086 is divided into two memory banks: odd bank and the even bank.

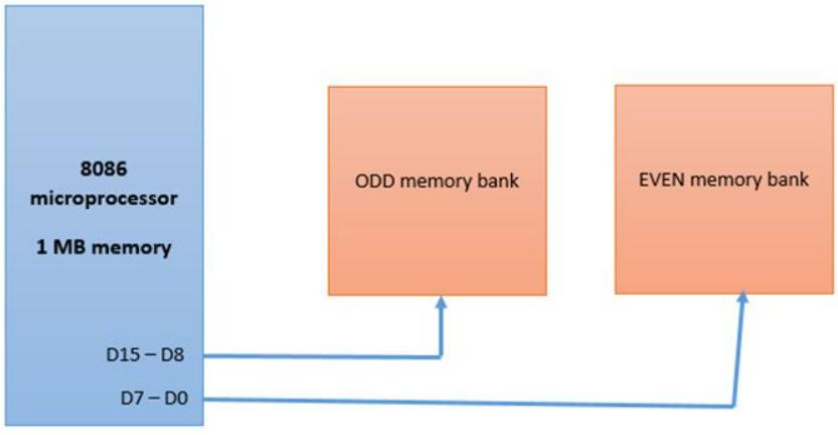

Figure 1: Memory organization in 8086 micro processor

The way in which data is read or written is decided by the value of BHE, and the last address bit, that is the A0 line. It is done in the following way:

$\overline{BHE}$	A0	Operation performed on memory
0	0	16 bits of data will be read or written into the memory
0	1	8 bits of data will be read/written into the odd memory bank
1	0	8 bits of data will be read/written into the even memory bank
1	1	No operation is performed

To read or write 8 bits of data, it would require only 1 CPU cycle, no matter the data is stored in any of the memory banks, but to read or write 16 bits of data, the BIU of the 8086 may require either 1 or 2 memory cycles depending upon whether the lower byte of word is located at even or odd memory address.

1. If the lower byte of the word is stored at even memory bank and the upper byte is stored at odd memory bank then the CPU will require only 1 memory cycle. So, it is better to store data in this way.

2. If the lower byte of the word is located at an odd memory address, then the CPU will require 2 memory cycles. The first memory cycle is required for accessing the lower byte of the word through the higher data bus, i.e. D15 to D8, and the second memory cycle is required for accessing the upper byte of the word through the lower data bus, i.e. D7 to D0.

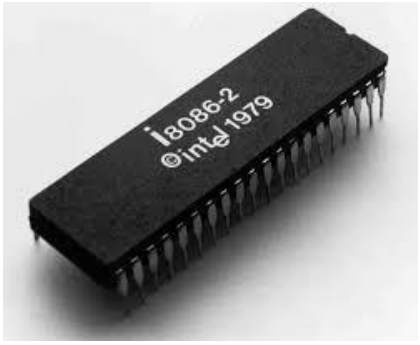

Figure 2: Microprocessor

Figure 3: Microprocessor kit

Figure 2 shows the image of microprocessor 8086. Microprocessor kit with all the additional interface is connected to the 8086 microprocessor is given in the figure 3. Figure 4 shows the assignment of the role to individual students. Students are assigned to address bus, BHE and A0 pins. Figure 5 shows the data collection from the memory as a small pocket.

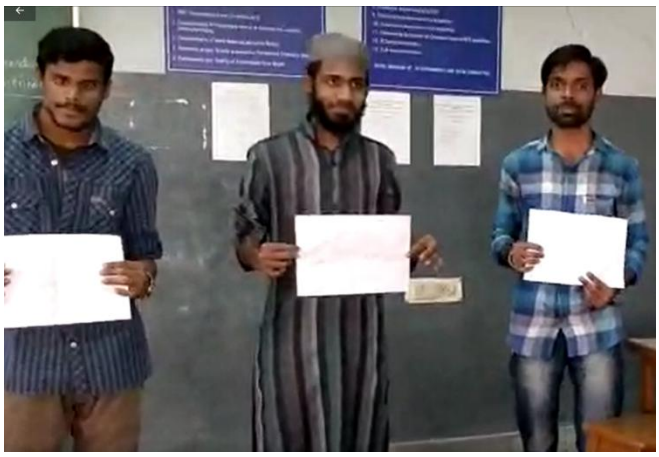

Figure 4: Students assigned their role

Figure 5: Data collection from the memory

Address and data transfer is depicted in the figure 6. The students in the classroom are shown in the figure 7.

Figure 6: Data transferring

Figure 7: Students in the Classroom

Outcome: Students understand the memory organization in the microprocessor and data transfer mechanism from the memory to microprocessor.

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