

Vidya Jyothi Institute of Technology

(Accredited by NAAC & NBA, Approved by AICTE New Delhi & Permanently Affiliated to JNTUH) Aziz Nagar Gate, C.B. Post, Hyderabad-500 075

B. Tech. III Year II Semester

| L | Τ | Р | С |
|---|---|---|---|
| 0 | 0 | 2 | 1 |

POWER ELECTRONICS AND SIMULATION LABORATORY

Course Code: A46289

- Course Outcomes: Upon the completion of Laboratory course, the student will be able to
 - CO1. Examine the characteristics of SCR, MOSFET, & IGBT, and analyze triggering circuits.
 - CO2. Analyze input and output characteristics of AC-DC converters.
 - CO3. Synthesize characteristics of Cycloconverters.
 - CO4. Examine characteristics of DC-DC Converters and Inverters.
 - CO5. Design of converters and inverters using P-Spice software.

List of Experiments

Any ten of the following experiments are required to be conducted.

- 1. Study of characteristics of SCR, MOSFET & IGBT.
- 2. Gate Firing Circuits for SCRs (R- Triggering, RC Triggering & UJT Triggering).
- 3. Single Phase AC voltage Controller with R & RL Loads.
- 4. Single Phase fully Controlled Bridge Converter with R& RL Loads.
- 5. DC Jones Chopper with R & RL Loads.
- 6. Single Phase Parallel Inverter with R& RL Loads.
- 7. Single Phase Cycloconverter with R& RL Loads.
- 8. Single Phase Series Inverter with R& RL Loads.
- 9. Single Phase Half controlled converter with R Load.
- 10. Simulation of single-phase full converter using RLE loads and single-phase AC voltage controller using RLE loads.
- 11. Simulation of resonant pulse commutation circuit and Buck Chopper.
- 12. Simulation of single phase Inverter with PWM control.

Head of + Department Department of Electrical & Electronics Enga

Vidya Jyothi Institute of Technology HYDERABAD-500 075. .

: 16 mgs

PRINCIPAL Vidya Jyothi Institute of Technology Himayatnagar (Vill), C.B. Post., Hyderabad-75.



Vidya Jyothi Institute of Technology (An Autonomous Institution) (Accredited by NAAC & NBA, Approved by AICTE New Delhi & Permanently Affiliated to JNTUH)

Aziz Nagar Gate, C.B. Post, Hyderabad-500 075

Correlation of COs with Experiments

| S.No. | Title of Experiment | COs Mapped |
|-------|---|------------|
| 1 | Study of characteristics of SCR, MOSFET & IGBT. | CO1 |
| 2 | Gate Firing Circuits for SCRs (R- Triggering, RC | CO1 |
| | Triggering & UJT Triggering). | |
| 3 | Single Phase AC voltage Controller with R & RL Loads. | CO2 |
| 4 | Single Phase fully Controlled Bridge Converter with R& | CO2 |
| | RL Loads. | |
| 5 | DC Jones Chopper with R & RL Loads. | CO4 |
| 6 | Single Phase Parallel Inverter with R& RL Loads. | CO4 |
| 7 | Single Phase Cycloconverter with R& RL Loads. | CO3 |
| 8 | Single Phase Series Inverter with R& RL Loads. | CO4 |
| 9 | Single Phase Half controlled converter with R Load. | CO2 |
| 10 | Simulation of single-phase full converter using RLE loads | CO2,CO5 |
| | and single-phase AC voltage controller using RLE loads. | |
| 11 | Simulation of resonant pulse commutation circuit and | CO4,CO5 |
| | Buck Chopper. | |
| 12 | Simulation of single phase Inverter with PWM control. | CO4,CO5 |



Vidya Jyothi Institute of Technology

(An Autonomous Institution)

(Accredited by NAAC & NBA, Approved by AICTE New Delhi & Permanently Affiliated to JNTUH) Aziz Nagar Gate, C.B. Post, Hyderabad-500 075

Programme Outcomes (POs)

Engineering Graduates will be able to:

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes

PSO1: Conceptualize electrical and electronics systems, employ control strategies for power electronics related applications to prioritize societal requirements.

PSO 2: Apply the appropriate techniques and modern engineering hardware and software tools in electrical engineering to engage in multi-disciplinary environments



Vidya Jyothi Institute of Technology (An Autonomous Institution) (Accredited by NAAC & NBA, Approved by AICTE New Delhi & Permanently Affiliated to JNTUH)

Aziz Nagar Gate, C.B. Post, Hyderabad-500 075

| | POWER ELECTRONICS & SIMULATION LAB | | | | | | | | | | | |
|-------------|------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-------------|------|-------|
| C328 | DO 1 | DOO | | | | | | | | | | DO 10 |
| | POI | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | POIT | PO12 |
| C328.1 | 3 | 2 | 2 | 2 | - | - | - | - | 3 | - | - | 3 |
| C328.2 | 3 | 3 | 3 | 2 | - | - | - | - | 3 | - | - | 3 |
| C328.3 | 3 | 3 | 3 | 2 | - | - | - | - | 3 | - | - | 3 |
| C328.4 | 3 | 3 | 3 | 2 | - | - | - | - | 3 | - | - | 3 |
| C328.5 | 3 | 3 | 3 | 2 | - | - | - | - | 3 | - | - | 3 |
| | 3 | 2.8 | 2.8 | 2 | - | - | - | - | 3 | - | - | 3 |
| | | | | | 00 | DOM | • | | | | | |

CO – PO Mapping

CO – PSO Mapping

| POWER EL | POWER ELECTRONICS AND SIMULATION LAB | | | | | |
|----------|--------------------------------------|------|--|--|--|--|
| C328 | PSO1 | PSO2 | | | | |
| C328.1 | 3 | - | | | | |
| C328.2 | 3 | - | | | | |
| C328.3 | 3 | - | | | | |
| C328.4 | 3 | - | | | | |
| C328.5 | 3 | 3 | | | | |
| | 3 | 3 | | | | |



DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Rubrics for Power Electronics and Simulation Laboratory Rubrics for Hardware based Experiments

Total Marks: 15M

| S. No. | Assessment Criteria | Excellent (80 – 100%) | Good (60-80%) | Average (Below 60%) |
|-----------|---|---|--|---|
| 1 | Theoretical Knowledge to perform the experiment (2M) | Student replied to all the questions posed by Laboratory teacher | Student replies to a minimum of 50% questions posed by the laboratory teacher | Student could not answer in the first session |
| | equipment required | Correctness in the rating and type of the equipment required | Correctness in the rating and type of equipment required with minor corrections | Student could not prepare the list of equipment required |
| 3 | Making the circuit connections as per the circuit diagram. (3 M) | Correctness of connections | Correctness of connections with minor corrections. | Unable to connect |
| 4 | Performing the experiment and tabulating the values (3 M) | Independent performance of the experiment with correct values | Performance of the experiment with teacher assistance | Unable to perform the experiment |
| 5 | Record book (based on calculations, results, graphs) (5 M) | Practical values matching with theoretical values/ Expected graph obtained. | Minor deviation in the practical values/ expected graph | Deviation of practical values with theoretical values / expected graph. |



Vidya Jyothi Institute of Technology

(An Autonomous Institution)

(Accredited by NAAC & NBA, Approved by AICTE New Delhi & Permanently Affiliated to JNTUH) Aziz Nagar Gate, C.B. Post, Hyderabad-500 075

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Rubrics for Power Electronics and Simulation Laboratory

Rubrics for Software/Simulation based Experiments

Total Marks: 15 M

| S. No | Assessment Criteria | Excellent (80 – 100%) | Good (60-80%) | Average (Below 60%) |
|----------|--|---|--|--|
| 1 | Theoretical Knowledge to perform the experiment (2M) | Student replied to all the questions posed by Laboratory teacher | Student replies to a minimum of 50% questions posed by the laboratory teacher | Student could not answer in the first session |
| 2 | Writing a program / simulation diagram of the experiment (3M) | Correctness in the rating and type of the equipment required | Correctness in the rating and type of equipment required with minor corrections | Student could not prepare the list of equipment required |
| 3 | Execution of the program / simulation (5 M) | Executed without errors | Partially Executed | Unable to run the program |
| 4 | Record book (calculations, results, plots) (5 M) | Simulation output matching with theoretical values/ Expected plot obtained. | Minor deviation in the simulation output/ expected plot | Deviation of simulation output with theoretical values / expected plot. |



Department of Electrical and Electronics Engineering

STUDENT PERFORMANCE EVALUATION TOTAL MARKS (75M)

EXTERNAL EVALUATION (50 Marks)

| Circuit Diagram | 10M |
|---------------------------------------|-----|
| Procedure write up | 10M |
| Experiment connections & observations | 10M |
| Calculations | 10M |
| Viva Voce | 10M |

INTERNAL EVALUATION (25 Marks)

| Day to day evaluation | 10M |
|-----------------------|-----|
| Record | 5M |
| Internal Exam | 10M |

LABORATORY MANUAL for Power Electronics and Simulation Lab

III Year B.Tech II Semester

Prepared by Mr. B. Rajesh and Mrs. P. Vaishnavi Devi, Assistant Professors, Department of Electrical and Electronics Engineering



VIDYA JYOTHI INSTITUTE OF TECHNOLOGY

(An Autonomous Institution) C.B.Post, Aziznagar, Hyderabad



POWER ELECTRONICS AND SIMULATION LAB

INDEX

| S.No. | Title | Page No. |
|-------|---|----------|
| 1 | Vision Mission of the Institute and Department | i |
| 2 | Course Outcomes and List of Experiments | ii |
| 3 | Correlation of COs with Experiments | iii |
| 4 | Program Outcomes and Program Specific Outcomes | iv |
| 5 | CO – PO and CO – PSO Mappings | v |
| | Experiments | |
| 6 | Study of characteristics of SCR, MOSFET &IGBT. | 1-8 |
| 7 | Gate Firing Circuits for SCRs (R- Triggering, RC Triggering & UJT | 9-13 |
| | Triggering). | |
| 8 | Single Phase AC voltage Controller with R & RL Loads. | 14-15 |
| 9 | Single Phase fully Controlled Bridge Converter with R& RL Loads. | 16-17 |
| 10 | DC Jones Chopper with R & RL Loads. | 18-19 |
| 11 | Single Phase Parallel Inverter with R& RL Loads. | 20-21 |
| 12 | Single Phase Cycloconverter with R& RL Loads. | 22-23 |
| 13 | Single Phase Series Inverter with R& RL Loads. | 24-25 |
| 14 | Single Phase Half controlled converter with R Load. | 26-27 |
| 15 | Simulation of single-phase full converter using RLE loads and single- | 28-31 |
| | phase AC voltage controller using RLE loads. | |
| 16 | Simulation of resonant pulse commutation circuit and Buck Chopper. | 32-33 |
| 17 | Simulation of single phase Inverter with PWM control. | 34-35 |

Vision of the Institution

- To develop into a reputed Institution at National and International level in Engineering, Technology and Management by generation and dissemination of knowledge through intellectual, cultural and ethical efforts with human values.
- To foster Scientific temper in promoting the world class professional and technical expertise.

Mission of the Institution

- To create state-of-the-art infrastructure facilities for optimization of knowledge acquisition.
- To nurture the students holistically and make them competent to excel in the global scenario.
- To promote R&D and consultancy through strong industry-institute interaction to address the societal problems.

Vision of the Department

• To become a reputed department in the impartation of professional and technical expertise in the field of Electrical and Electronics Engineering.

Mission of the Department

- Imparting Quality Technical Education by provision of state-of-the-art learning facilities.
- Preparing the students to think innovatively and find effective solutions to address engineering and societal problems with a multi-disciplinary approach maintaining continuous industry interaction.
- Encouraging team work and preparing the students for lifelong learning with ethical responsibility for a successful professional career.

Programme Educational Outcomes (PEOs)

PEO1: To provide the students with a sound foundation in the mathematics, science and engineering fundamentals necessary to become employable.

PEO2: Graduates should apply their technical knowledge to take up higher responsibilities in industry, academics and create innovative ideas in the field of Electrical and Electronics Engineering.

PEO3: Equip graduates with communication skills, leadership qualities with ethical values, team work with multi-disciplinary approach and zeal to provide solutions for engineering and societal problems.

B. Tech. III Year II Semester

Course Code: A46289

Course Outcomes: Upon the completion of Laboratory course, the student will be able to

- CO1. Examine the characteristics of SCR, MOSFET, & IGBT, and analyze triggering circuits.
- CO2. Analyze input and output characteristics of AC-DC converters.
- CO3. Synthesize characteristics of Cycloconverters.
- CO4. Examine characteristics of DC-DC Converters and Inverters.
- CO5. Design of converters and inverters using P-Spice software.

List of Experiments

Any ten of the following experiments are required to be conducted.

- 1. Study of characteristics of SCR, MOSFET & IGBT.
- 2. Gate Firing Circuits for SCRs (R- Triggering, RC Triggering & UJT Triggering).
- 3. Single Phase AC voltage Controller with R & RL Loads.
- 4. Single Phase fully Controlled Bridge Converter with R& RL Loads.
- 5. DC Jones Chopper with R & RL Loads.
- 6. Single Phase Parallel Inverter with R& RL Loads.
- 7. Single Phase Cycloconverter with R& RL Loads.
- 8. Single Phase Series Inverter with R& RL Loads.
- 9. Single Phase Half controlled converter with R Load.
- 10. Simulation of single-phase full converter using RLE loads and single-phase AC voltage controller using RLE loads.
- 11. Simulation of resonant pulse commutation circuit and Buck Chopper.
- 12. Simulation of single phase Inverter with PWM control.





| S.No. | Title of Experiment | COs Mapped |
|-------|--|-------------------|
| 1 | Study of characteristics of SCR, MOSFET &IGBT. | CO1 |
| 2 | Gate Firing Circuits for SCRs (R- Triggering, RC Triggering & UJT Triggering). | C01 |
| 3 | Single Phase AC voltage Controller with R & RL Loads. | CO2 |
| 4 | Single Phase fully Controlled Bridge Converter with R& | CO2 |
| | RL Loads. | |
| 5 | DC Jones Chopper with R & RL Loads. | CO4 |
| 6 | Single Phase Parallel Inverter with R& RL Loads. | CO4 |
| 7 | Single Phase Cycloconverter with R& RL Loads. | CO3 |
| 8 | Single Phase Series Inverter with R& RL Loads. | CO4 |
| 9 | Single Phase Half controlled converter with R Load. | CO2 |
| 10 | Simulation of single-phase full converter using RLE loads | CO2,CO5 |
| | and single-phase AC voltage controller using RLE loads. | |
| 11 | Simulation of resonant pulse commutation circuit and | CO4,CO5 |
| | Buck Chopper. | |
| 12 | Simulation of single phase Inverter with PWM control. | CO4,CO5 |

Correlation of COs with Experiments

Sec.

×

Programme Outcomes (POs)

Engineering Graduates will be able to:

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes

PSO1: Conceptualize electrical and electronics systems, employ control strategies for power electronics related applications to prioritize societal requirements.

PSO 2: Apply the appropriate techniques and modern engineering hardware and software tools in electrical engineering to engage in multi-disciplinary environments

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

iv

in a

.



CO – PO Mapping

| ~~~~ | POWER ELECTRONICS & SIMULATION LA | | | | | | ON LAI | B | | | | |
|--------|-----------------------------------|-----|-----|-----|-----|-----|--------|-----|-----|------|------|------|
| C328 | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
| C328.1 | 3 | 2 | 2 | 2 | - | - | - | _ | 3 | - | - | 3 |
| C328.2 | 3 | 3 | 3 | 2 | - | - | - | | 3 | - | - | 3 |
| C328.3 | 3 | 3 | 3 | 2 | | - | - | - | 3 | - | - | 3 |
| C328.4 | 3 | 3 | 3 | 2 | - | - | - | - | 3 | - | | 3 |
| C328.5 | 3 | 3 | 3 | 2 | - | - | - | - | 3 | - | - | 3 |
| | 3 | 2.8 | 2.8 | 2 | - | - | - | - | 3 | - | - | 3 |

CO – PSO Mapping

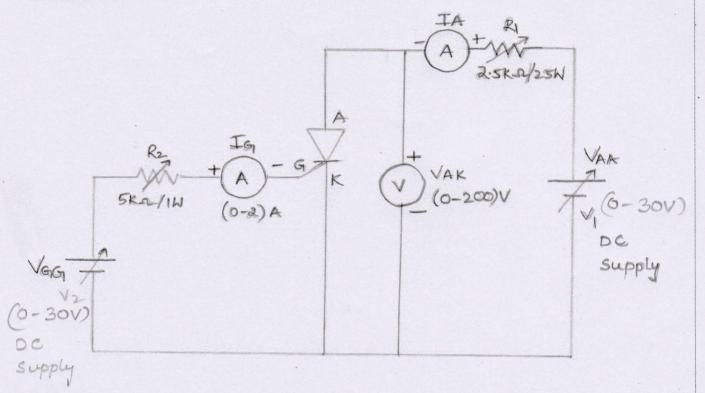
| C328 | PSO1 | PSO2 |
|--------|------|------|
| C328.1 | 3 | - |
| C328.2 | 3 | - |
| C328.3 | 3 | - |
| C328.4 | 3 | - |
| C328.5 | 3 | 3 |
| | 3 | 3 |

.

V

1.a) STATIC CHARACTERISTICS OF SCR

CIRCUIT DIAGRAM:





Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

1. a) STUDY OF CHARACTERISTICS OF SCR

AIM: To plot V- I characteristics of SCR and find the latching and holding currents of SCR THEORY: Silicon Controlled Rectifier (SCR) is a four layered three junction P N P N semiconductor switching device. It has three terminals named as anode, cathode and gate. SCR is made up of silicon. It has very low resistance in the forward direction and high resistance in the reverse direction. It is a unidirectional device.

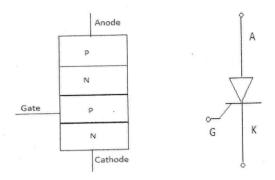


Fig 1.1: SCR and its symbol

Static V-I characteristic of SCR:

SCR can be operated in three modes.

- 1. Reverse blocking mode
- 2. Forward blocking mode (Off state)
- 3. Forward conduction mode (On state)

1. Reverse Blocking Mode:

When the cathode of SCR is made positive with respect to anode, SCR is reverse biased. Junctions J1 and J2 are reverse biased where junction J3 is forward biased. The device behaves as if two diodes are connected in series with reverse voltage applied across them.

A small leakage current of the order of few milli Amperes only flows. As SCR is reverse biased and in blocking mode, it is called as reverse blocking mode of operation. Now if the reverse voltage is increased, at a critical breakdown level called reverse breakdown voltage V_{BR} , an avalanche occurs at J1 and J3 and the reverse current increases rapidly through the SCR. This results in SCR damage as junction temperature may exceed its maximum temperature rise.

2. Forward Blocking Mode:

When anode is positive with respect to cathode, with gate circuit open, SCR is said to be forward biased mode. Then junction J1 and J3 are forward biased and J2 is reverse biased. As

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

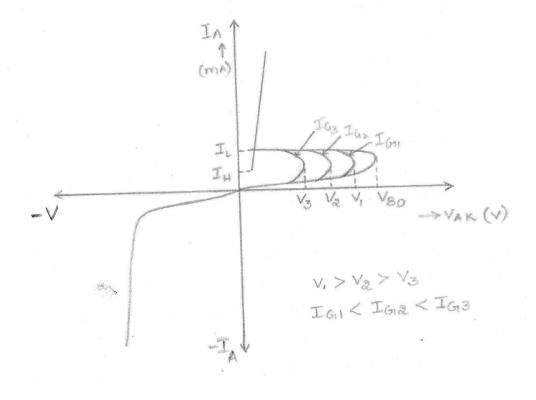
TABULAR COLUMN:

| IG(mA) | I _A (mA) | Vak(V) | IG(mA) | I _A (mA) | Vak(V) | IG(mA) | I _A (mA) |
|--------|---------------------|---------------|--------------------------|--|---|--|--|
| | | | н ²¹ М | | | | |
| | | | | e de la | | | |
| | | | | | | | |
| | × | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | - | | - | |
| | IG(mA) | IG(MA) IA(MA) | IG(MA) IA(MA) VAK(V) | IG(mA) IA(mA) VAK(V) IG(mA) IG IG IG IG IG IG <td>IG(mA) IA(mA) VAK(V) IG(mA) IA(mA) I I I III IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII</td> <td>IG(mA) IA(mA) VAK(V) IG(mA) IA(mA) VAK(V) I I I IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII</td> <td>IG(mA) IA(mA) VAK(V) IG(mA) IA(mA) VAK(V) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA)</td> | IG(mA) IA(mA) VAK(V) IG(mA) IA(mA) I I I III IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII | IG(mA) IA(mA) VAK(V) IG(mA) IA(mA) VAK(V) I I I IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII | IG(mA) IA(mA) VAK(V) IG(mA) IA(mA) VAK(V) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) IG(mA) |

 $I_L = (mA) \qquad I_H = _____$

(mA)

MODEL GRAPH:





Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology



the forward voltage is increased, junction J2 will have an avalanche breakdown at a voltage called forward break over voltage V_{BO} . When forward voltage is less then , SCR offers high impedance. Thus an SCR acts as an open switch in forward blocking mode.

3. Forward Conduction Mode:

In this mode of SCR conducts current from anode to cathode with a very small voltage drop across it. An SCR can be brought from forward blocking mode to forward conducting mode:

- 1. By exceeding the forward break over voltage.
- 2. By applying a gate pulse between gate and cathode.

During forward conduction mode of operation, SCR is in on state and behaves like a closed switch. Voltage drop is of the order of 1 to 2mV. This small voltage drop is due to resistance drop across the four layers of the device.

Latching current: The latching current is the minimum value of anode current which must be attained by the SCR to turn ON.

Holding current: It is the minimum value of anode current below which the SCR turns of if it falls, the SCR will turn OFF.

APPARATUS:

1. SCR characteristics study unit.

2. Meters

- a. Voltmeter (0-20) V 1 No.
- b. Ammeter (0-2) A 1 No.
- c. Ammeter (0-200) mA 1 No.
- 3. Patch cords

PROCEDURE:

1. Make the connections as per the circuit diagram.

2. Switch ON the main supply and keep the voltages V1 &V2 at minimum position initially.

- 3. Vary V_1 and set the voltage V_{AK} to 10V.
- 4. Slowly vary V_2 in steps and note down I_G , I_A and V_{AK} values.
- 5. Vary V₂ till V_{AK} suddenly drops down. This indicates that the SCR started conduction.
- 6. Repeat the same procedure for $V_{AK} = 15V$ and 20V.



7. Draw the graph V_{AK} vs I_A for different values of I_G .

Procedure to find Latching current:

11111

1. Apply about 20 V between Anode and Cathode by varying V1.

2. Keep the load potentiometer R1 at minimum position.

3. The device must be in the OFF state with gate open.

4. Gradually increase Gate voltage - V2 till the device turns ON.

5. The minimum anode current at which the SCR turns ON is the latching current.

6. Note down the latching current.

Procedure to find Holding current:

1. Increase the load current from the latching current level by increasing V1.

2. Open the gate switch permanently. The SCR must be fully ON.

3. Now start reducing the load current gradually by adjusting R1. If the SCR does not turns OFF even after the R1 at maximum position, then reduce V1.

4. Observe when the device goes to Blocking mode. The load current through the device at this instant, is the holding current of the device.

5. Note down the holding current.

RESULT: The static characteristics (V I Characteristics) of SCR are studied and latching and holding currents of the SCR are found.

Power Electronics and Simulation Laboratory 1 b) CHARACTERISTICS OF MOSFET **CIRCUIT DIAGRAM**: (0-200)m NDD DC Supply UDS 10-200 (nS (0-30V), VGG Supply (0-20)V

Fig 1.6

TABULAR COLUMN :

Output Characteristics :

| | $V_{GS} = 2V$ | | $V_{GS} = 2.7$ | V | $V_{\rm GS}=2.9$ | V |
|-------|---------------------|---------------------|---------------------|---------------------|------------------|---------------------|
| S.NO. | V _{DS} (V) | I _D (mA) | V _{DS} (V) | I _D (mA) | VDS (V) | I _D (mA) |
| Bry. | 2 | _ | | | | |
| | | | | | | 5 |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

.

1. b) STUDY OF CHARACTERISTICS OF MOSFET

AIM: To plot the output and transfer characteristics of MOSFET.

THEORY:

A power MOSFET has three terminals called Drain (D), Source(S) and Gate(G).

MOSFET is a voltage controlled device. It's operation depends on the flow of majority carriers

only. MOSFET is a unipolar device.

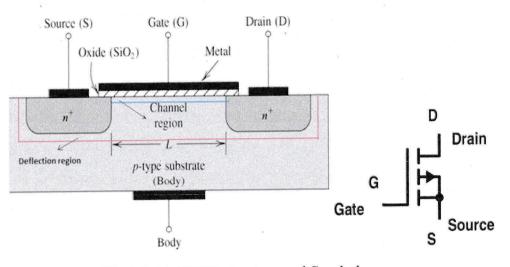


Fig 1.2: MOSFET structure and Symbol

Power MOSFETs are of two types, n-channel enhancement MOSFET and p-channel enhancement MOSFET. Out of these two types, n-channel enhancement MOSFET is commonly used because of higher mobility of electrons.

The IGBT does not conduct when the gate circuit is open. When gate is made positive with respect to source, an electric field is established. Then negative charges are induced in the p-substrate below SiO2 layer. The n-channel current flows from drain to source. If V_{GS} is made more positive, n-channel expands and therefore, more current flows from D to S. The drain current I_D is enhanced by the gradual increase of gate voltage. Hence the name enhancement MOSFET is used.

Output Characteristics: Power MOSFET output characteristics indicate the variation of drain current I_D as a function of drain-source voltage V_{GS} . For low values of V_{DS} , the graph between $I_D \& V_{DS}$ is almost linear. This indicates a constant value of on-resistance

$R_{DS} = V_{DS} / I_D.$

For given V_{GS} , if V_{DS} is increased, output characteristic is relatively flat indicating that drain current is nearly constant.

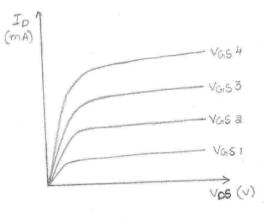
Transfer Characteristics :

.

| | $V_{\rm DS} = 2.5 V$ | | | | |
|-------|----------------------|---------------------|--|--|--|
| S.NO. | V _{GS} (V) | I _D (mA) | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| e. | | | | | |

MODEL GRAPHS :

Output Characteristics:





Transfer Characteristics:

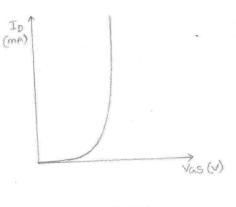


Fig 1.8



Transfer Characteristics: These characteristics show the variation of drain current I_D as a function of gate-source voltage V_{GS} . In the transfer characteristic, the device turns off if VGS is decreased below the threshold voltage V_{GST} .

APPARATUS:

- 1. MOSFET characteristics study unit.
- 2. Meters
 - a. Voltmeter (0-20) V 1 No.
 - b. Voltmeter (0-200) V 1 No.
 - c. Ammeter (0-200) mA-1 No.
- 3. Patch cords.

(a) Drain /Output Characteristics:

- 1. Make the connections as per the circuit diagram.
- 2. Vary the supply V2 and adjust $V_{GS} = 2V$.
- 3. Vary the supply V1 in steps and note down the values of $V_{DS} \& I_D$
- 4. Repeat the procedure for different values of V_{GS} (at least two different values of V_{GS})
- 5. Plot the graph of V_{DS} vs I_D for different values of V_{GS} .

(b) Transfer Characteristics:

- 1. Set V_{DS} to 2.5V by varying V1.
- 2. Vary V2 in steps, note down V_{GS} and I_D
- 3. Plot the characteristics V_{GS} vs I_D .

RESULT: The Output and Transfer characteristics of MOSFET are plotted and studied.

1 c) CHARACTERISTICS OF IGBT

CIRCUIT DIAGRAM:

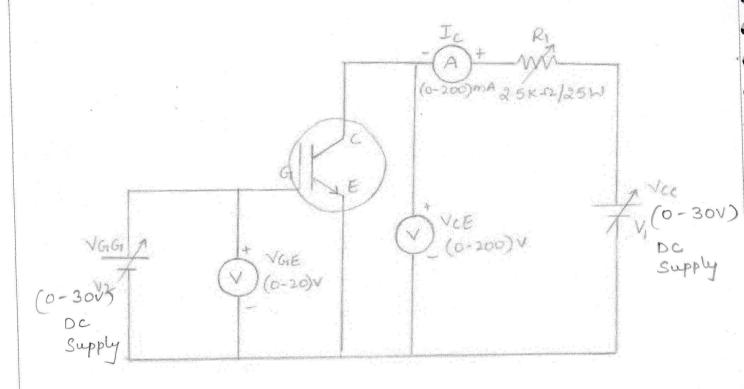


Fig 1.3

TABULAR COLUMN:

Output Characteristics:

| | $V_{GE} = 4V$ | | $V_{GE} = 5 V$ | | $V_{GE} = 5.2$ | V |
|-------|---------------|---------|----------------|---------|----------------|---------|
| S.NO. | VCE (V) | Ic (mA) | VCE (V) | Ic (mA) | VCE (V) | Ic (mA) |
| then | | | | | | |
| | | | | | * 2 | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

.

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

Ō

1. c) STUDY OF CHARACTERISTICS OF IGBT AIM: To plot the output and transfer characteristics of IGBT.

THEORY:

An IGBT has three terminals called Collector, Gate and Emitter. When gate is positive with respect to emitter and with gate-emitter voltage more than threshold voltage of IGBT, an n-channel is formed in the p-regions as in a power MOSFET. This n-channel short circuits the n-region with n+ emitter regions. An electron movement in the n-channel, in turn, causes substantial hole injection from pf substrate layer into the epitaxial n- layer. Eventually, a forward current is established. The three layers p+, n- and p constitute a pnp transistor with p+ as, emitter, n- as base and p as collector. Also n-, p and n+ layers constitute npn transistor as shown in below fig 1.3.

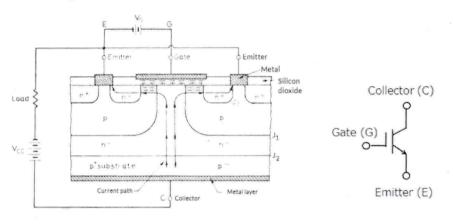


Fig 1.3: IGBT Structure and Symbol

The output characteristics of an IGBT are plot for collector current IC versus collectoremitter voltage VCE for various values of gate-emitter voltages. The output of IGBT is controlled by gate emitter voltage VGE. Hence IGBT is a voltage-controlled device.

The transfer characteristic of an IGBT is a plot of collector current IC versus gateemitter voltage VGE. This characteristic is identical to that of power MOSFET. When VGE is less than the threshold voltage VGET, IGBT is in off-state. When the device is off, junction J2 blocks forward voltage and in case reverse voltage appears across collector and emitter, junction J1 blocks it.

APPARATUS:

1. IGBT characteristics study unit.

2. Meters

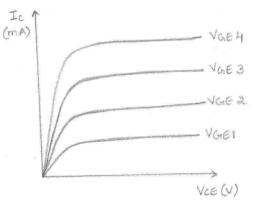
- a. Voltmeter (0-20)V 1 No.
- b. Voltmeter (0-200)V 1 No.
- c. Ammeter (0-200)mA 1 No.
- 3. Patch cords.

Transfer Characteristics :

| | $V_{CE} = 5V$ | |
|-------|---------------------|---------------------|
| S.NO. | V _{GE} (V) | I _C (mA) |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

MODEL GRAPHS:

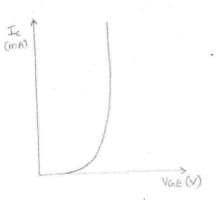
Output Characteristics :





٠

Transfer Characteristics:





PROCEDURE:

(a) Output Characteristics:

1. Make the connections as per the circuit diagram.

2. Vary V2 and set V_{GE} to 4V.

3. Vary V1 in steps and note down V_{CE} and I_{C} for each step.

4. Plot the graph of I_C vs V_{CE} for different values of VGE.

(b) Transfer Characteristics:

- 1. Vary V1 and set VCE at 5V.
- 2. Vary V2 in steps and note down V_{GE} and I_{C}

3. Plot a graph for V_{GE} vs I_C .

RESULT: The output and transfer characteristics of IGBT are plotted and studied.

GATE FIRING CIRCUITS

CIRCUIT DIAGRAM:

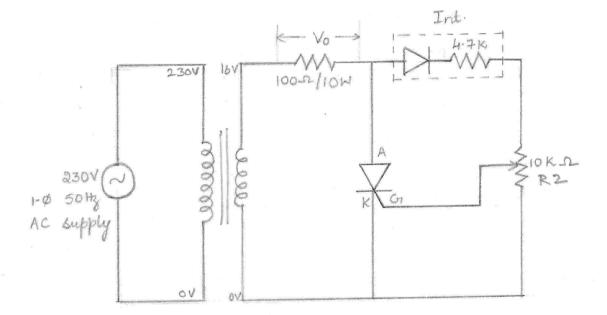


Fig 2.1

TABULAR COLUMN:

| S.No. | Firing angle (a) | Load voltage (V) |
|-------|------------------|------------------|
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

•



9

2. GATE FIRING CIRCUITS OF SCR

1. R TRIGGERING CIRCUIT

AIM: To study the switching control of SCR with R triggering circuit.

THEORY:

The conventional gate triggering circuits used to turn ON an SCR are:

- 1. Resistance triggering (amplitude control)
- 2. RC triggering (Phase control)
- 3. UJT triggering (Phase control)
- 4. Ramp and pedestal triggering
- 5. DC triggering.
- 6. Digital triggering schemes.
- 7. Microprocessor controlled triggering schemes.
- 8. Light triggering in LASCR.

Resistance Triggering: This is the simplest method of turning on an SCR in phase control circuit. A resistance of suitable value is connected between anode and gate through a diode. Whenever anode voltage is positive, current flows from gate to cathode circuit through this resistance. Hence SCR turns ON. But the gate current will remain as long as the anode to cathode voltage is positive. But the trigger angle can be controlled only from 0 to π /2 of the applied voltage. V_{GK} can be adjusted with R₂ but its phase positive is same as that of the AC supply voltage. Hence if SCR does not turn on at π /2, it cannot be turned on after π /2 since the magnitude of the voltage will decrease after this instant.

Load voltage $V_{DC} = \frac{Vm(1+Cos\alpha)}{2\pi}$

APPARATUS:

- 1. SCR Triggering module.
- 2. C.R.O.
- 3. Patch cords.
- 4. Multimeter

PROCEDURE:

- 1. Make the connections as per the circuit diagram.
- 2. Switch ON the supply.
- 3. Set the potentiometer to a particular position and observe the waveforms of VIN, Vo,

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

TABULAR COLUMN :

| S.No. | Firing angle (a) | Load voltage (V) |
|---------------------------------------|------------------|------------------|
| | | |
| <u></u> | | |
| | | |
| · · · · · · · · · · · · · · · · · · · | | × |
| | | |

| S.No. | Firing angle (α) | Load voltage (V) | | |
|-------|------------------|------------------|--|--|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

the second

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

•



 V_T , on the C.R.O. and note down the corresponding waveforms.

4. Vary the potentiometer in steps and note down the firing angle and the corresponding load voltage using multimeter.

RESULT: The switching control of SCR with R-triggering is observed and studied.

2 b) RC TRIGGERING

CIRCUIT DIAGRAM: RC HALF WAVE TRIGGERING

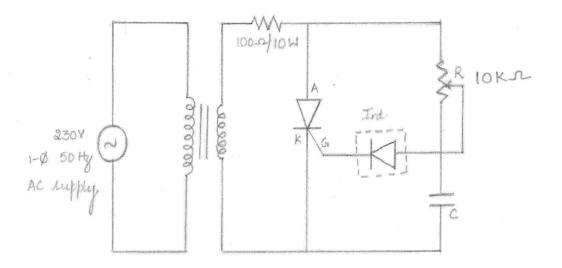


Fig 2.3

RC FULL WAVE TRIGGERING

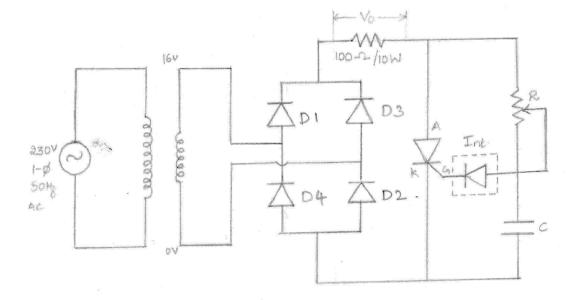


Fig 2.4

.

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology



2 b) RC TRIGGERING

AIM: To study the phase control of SCR by RC triggering.

THEORY:

In case of resistance triggering, the firing angle of the SCR can be varied from 0 to 90° only. Hence resistance triggering cannot not be employed in practice as the output voltage cannot be varied over a wide range (i.e., 0 to Vm / π in case of half wave and 0 to 2Vm / π in case of full wave).

To overcome the above limitations, Resistance and Capacitance (RC) triggering is employed so as to vary the triggering angle of SCR over the complete range 0 to 180°. RC triggering is very cheap and reliable for low voltage phase controlled circuits.

RC circuit helps to adjust the position of gate to cathode voltage as the voltage across the capacitor lags the current through it by 90°, by varying R, the phase angle w.r.t., applied voltage can be adjusted. Hence the triggering angle α can be varied over a wide range from 0 to 180°. By varying R, we can vary the triggering angle α . The load voltage can be obtained from $V_{DC} = \frac{Vm(1+Cos\alpha)}{2\pi}$

APPARATUS:

- 1. SCR Triggering module.
- 2. C.R.O.
- 3. Patch cords.
- 4. Multimeter.

PROCEDURE:

1. Make the connections as per the circuit diagram.

- 2. Switch ON the module.
- 2. Set the potentiometer to a particular position and observe the waveforms of V_{IN}, V_O, V_T, V_C on the C.R.O. and note down the corresponding waveforms.
- 3. Vary the potentiometer in steps and note down the corresponding load voltage using multimeter.

RESULT: The Phase control of SCR with RC triggering is studied.

2.c) UJT TRIGGERING CIRCUIT.

CIRCUIT DIAGRAM :

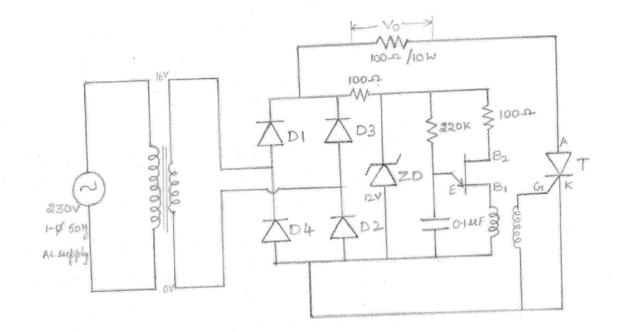


Fig 2.2

TABULAR COLUMN:

| S.No. | Firing angle (a) | Load voltage (V) |
|--------|------------------|------------------|
| | | |
| | | |
| 1947 - | | |
| Б Т | | |
| | | |
| | | |
| | | |
| | | |

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology



2. c) UJT TRIGGERING CIRCUIT

AIM: To study triggering control of SCR using UJT triggering circuit. **THEORY:**

Uni Junction Transistor (UJT) is a three terminal device with two bases (B1 and B2) and an Emitter (E) as shown in fig 2.1. Output pulses of variable time period are possible by suitably increasing the emitter to base voltage from valley voltage level to peak level either by employing a constant current source or by charging a capacitor by a resistor. The RC network can be easily employed to obtain output pulses, since the time period is fixed by RC circuit through the capacitor voltage V_C. The output pulses derived from the capacitor can be observed in fig 2.2.

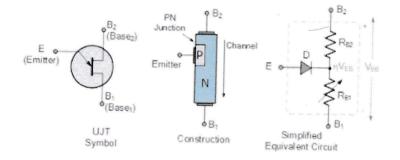
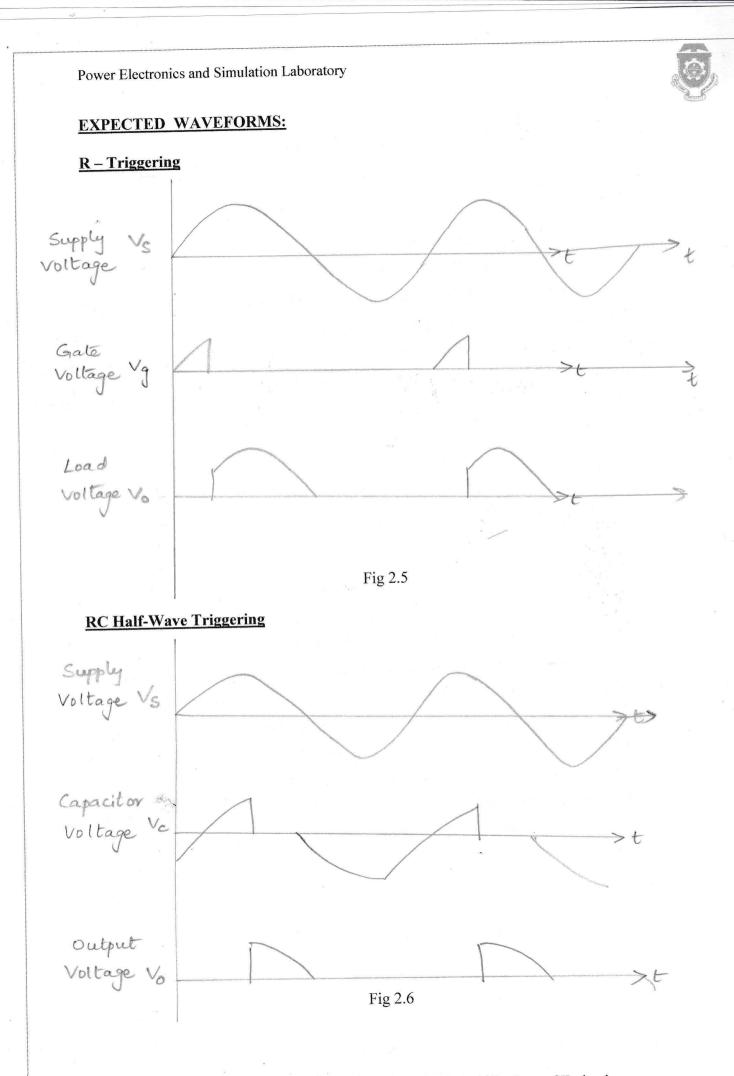


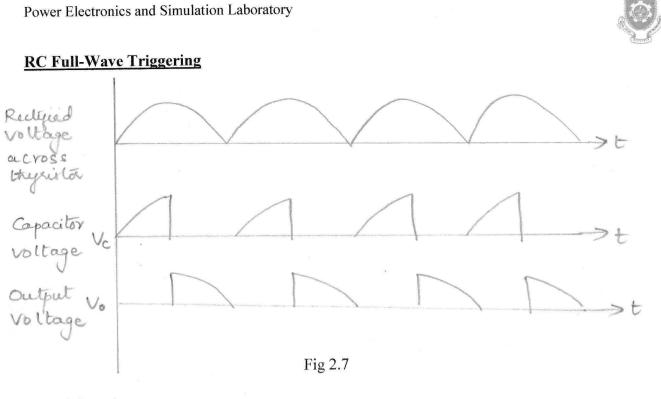
Fig 2.1: UJT Symbol, Structure and simplified equivalent circuit

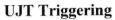
In phase controlled rectifier circuit, trigger pulses to SCR must be synchronized or phase locked with the AC supply frequency. This helps constant DC output voltage across the load for a specified triggering angle. On the other hand, if synchronization or phase locking is not achieved, then even for a minute variation in AC supply frequency, triggering angle of SCR varies from instant to instant, resulting in variation in DC output voltage across the load. To overcome this problem, the supply voltage to UJT circuit is derived from the AC mains using step down transformer, rectifier and Zener diode.

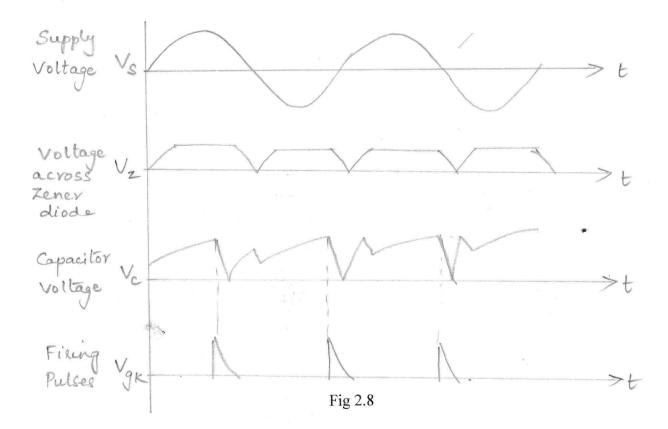


Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

•







Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology



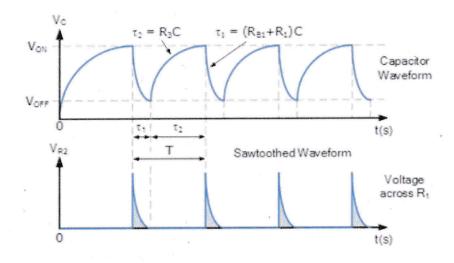


Fig 2.2: UJT Oscillator Waveforms

The rectifier circuit converts AC supply available at transformer secondary into full wave DC voltage. The DC voltage is clipped to the required DC voltage using a zener diode. The series resistance R_S limits the current through the zener diode. The clipped voltage V_Z is applied to the RC charging network and also to the UJT circuit. Depending on the resistance R and capacitance of C, trigger pulses can be obtained across isolation pulse transformer connected to base1. These pulses can be used to trigger SCRs. For SCRs of higher rating, this small pulse is amplified using a pulse amplifier and then by connecting across gate and cathode of the SCR.

APPARATUS:

- 1. SCR Triggering module.
- 2. C.R.O.
- 3. Patch cords.
- 4. Multimeter.

PROCEDURE:

- 1. Make the connections as per the circuit diagram.
- 2. Switch ON the module.
- 3. Set the potentiometer to a particular position and observe the waveforms of V_{IN} , V_O , V_T , V_C on the C.R.O. and note down the corresponding waveforms.
- 4. Vary the potentiometer in steps and note down the corresponding load voltage using multimeter.

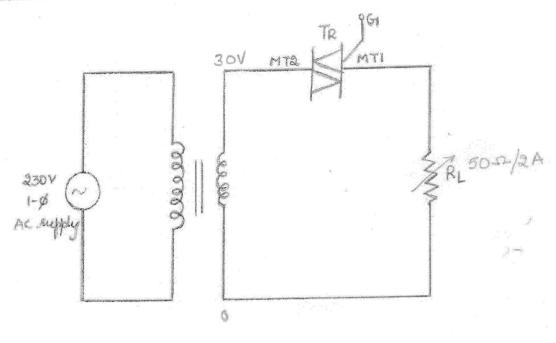
RESULT: The UJT triggering circuit to trigger an SCR is connected and the phase control of SCR using UJT is studied.

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

SINGLE PHASE AC VOLTAGE CONTROLLER.

CIRCUIT DIAGRAM:

Sin.





3. SINGLE PHASE AC VOLTAGE CONTROLLER WITH R AND RL LOADS

AIM: To obtain the output of Single phase AC Voltage Controller with R & RL load by implementing phase control technique.

THEORY:

AC Voltage Controller converts fixed alternating voltage to variable alternating voltage without change in frequency. The output of AC Voltage controller is controlled by Phase control technique. AC Voltage controller can be constructed using two antiparallel connected SCRs or a TRIAC. The arrangement of SCRs and TRAIC for the respective circuits can be understood from the following circuits.

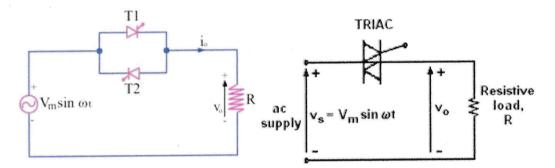


Fig 3: Single Phase AC Voltage Controllers with anti parallel SCRs and TRIAC

In the first circuit with two antiparallel SCRs, T1 conducts for the positive half cycle and T2 conducts for negative half cycle.

In the second circuit, TRIAC conducts for both the half cycles of AC supply. Therefore, for the firing angle α symmetrical AC voltage is available across the load. The load voltage is given by

$$V_{\rm O} = \frac{Vm}{\sqrt{2}} \left[\frac{1}{\pi} \left\{ (\pi - \alpha) + \frac{Sin2\alpha}{2} \right\} \right]^{\frac{1}{2}}$$

The voltage control of AC Voltage controller can be done by simply adjusting the firing angle of the SCRs or TRIAC by using phase control. The output can be controlled from 0 to maximum value for both the half cycles.

APPARATUS:

- 1. Single Phase AC Voltage Controller Unit.
- 2. Loading Rheostat (50 Ω /2A)
- 3. Loading Inductor (0-150 mH/2A)
- 4. Digital Multimeter.
- 5. C.R.O.
- 6. Patch cords.

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

TABULAR COLUMN:

For R Load:

Vm = _____ Volts

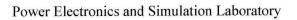
| S.No. | Firing Angle a (deg) | VL(V) |
|-------|----------------------|-------|
| 1 | 180 | |
| 2 | 150 | |
| 3 | 120 | |
| 4 | 90 | |
| 5 | 60 | |
| 6 | 30 | |
| 7 | 0 | |

For RL Load :

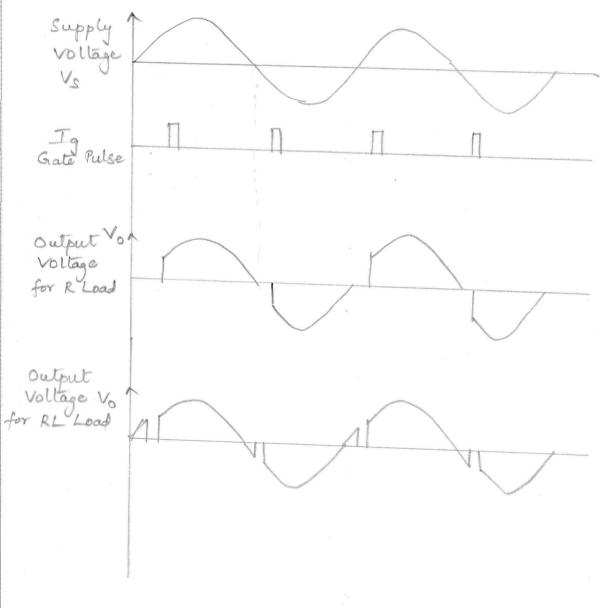
Vm =_____ Volts.

Hica.

| S.No. | Firing Angle α (deg) | VL(V) |
|-------|----------------------|-------|
| 1 | 180 | |
| 2 | 150 | |
| 3 | 120 | |
| 4 | 90 | |
| 5 | 60 | |
| 6 | 30 | |
| 7 | 0 | |









Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

PROCEDURE:

- 1. Connect the circuit as per the circuit diagram.
- 2. Switch ON the mains supply to the unit.
- 3. The firing angle of the switching circuit can be varied in steps and the corresponding firing angle, Input voltage, Output voltage, SCR/TRIAC Voltage waveforms can be recorded from the C.R.O.
- 4. The load voltage is measured using a multimeter.
- 5. Then connect an Inductive load in series to the resistive load.
- 6. Repeat the above steps for AC Voltage controller with RL Load.

RESULT: The operation of a Single Phase AC Voltage Controller is observed and its control is output waveforms are obtained for R & R L Loads.

SINGLE PHASE FULLY CONTROLLED BRIDGE CONVERTER.

CIRCUIT DIAGRAM:

thing.

a.A

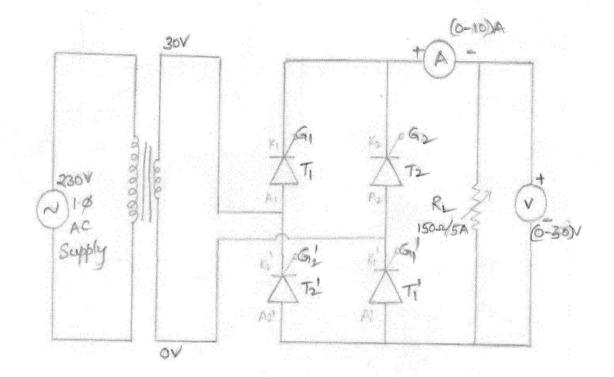


Fig 4.1

4. SINGLE PHASE FULLY CONTROLLED BRIDGE CONVERTER WITH R& RL LOADS

AIM: To obtain the output of Single phase Single Phase fully controlled converter with R & RL loads.

THEORY:

A Single Phase fully controlled converter converts Single phase AC supply to DC Supply. The circuit of the converter is as shown in the circuit diagram.

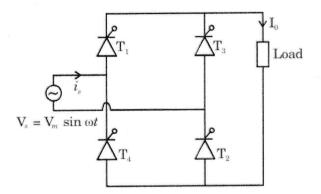


Fig 4.1: Single Phase Fully Controlled Converter

Full Controlled Bridge Converter with R Load:

During positive half cycle, thyristors T_1 and T_2 are triggered simultaneously through independent isolated pulse transformers. The pair of SCR's conduct up to π . SCR T_3 & SCR T_4 are triggered in the next half cycle with another pair of isolated pulse transformers.

Full Controlled Bridge Converter with RL load :

During positive half cycle, thyristors $T_1 \& T_2$ are forward biased and when these 2 thyristors are fired simultaneously, at $\omega t = \alpha$. the load is connected to the input supply through $T_3 \& T_4$. Due to inductive load, $T_1 \& T_2$ will continue to conduct beyond $\omega t = \pi$, even though the input voltage is already negative. During negative half-cycle of the input voltage, thyristor $T_3 \& T_4$ are forward biased, and firing of thyristors $T_3 \& T_4$ will apply the supply voltage across the load. Due to inductive load, T3 & T4 will continue to conduct beyond $\omega t = 2\pi$, even though the input voltage is already positive.

During the period from α to π , the input voltage V_S and input current are positive and the current flows from the supply to the load. The converter is said to be operated in rectification mode. During the period from π to π + α , the input voltage V_S is negative and the

TABULAR COLUMN:

For R Load:

Vm = _____ Volts.

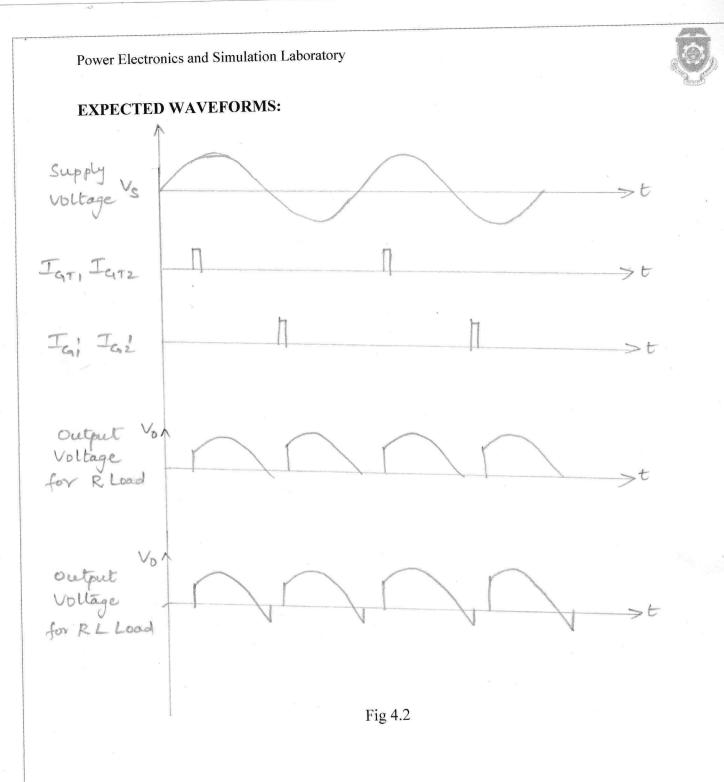
| S.No. | Firing Angle α (deg) | V _L (V) | IL (A) | $V_{\rm L} = \frac{Vm(1 + \cos \alpha)}{\pi}$ |
|-------|----------------------|---|--------|---|
| 1 | 180 | | | |
| 2 | 150 | | | |
| 3 | 120 | 4 607 | | |
| 4 | 90 | | | |
| 5 | 60 | | | |
| 6 | 30 | | | |
| 7 | 0 | 0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | | 1 |

For RL Load:

Vm =_____ Volts.

| S.No. | Firing Angle a (deg) | VL(V) | IL(A) | $V_L = V_m (1 + \cos \alpha) / \pi$ |
|-------|----------------------|---|-------|-------------------------------------|
| 1 | 180 | | | |
| 2 | 150 | | | 2 P |
| 3 | 120 | | | |
| 4 | 90 | | | |
| 5 | 60 | u da compañía de la c | | |
| 6 | 30 | | | |
| 7 | 0 | | | |

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology



Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

.

Him



input current I_S is positive and there will be reverse power flow from the load to the supply. The converter is said to be operated in inversion mode.

APPARATUS:

- 1. Single phase fully controlled bridge converter power unit
- 2. Single phase fully controlled bridge converter firing unit
- 3. Single phase Isolation transformer (0-230)V/5A with tappings.
- 4. Loading Rheostat $150\Omega/5A$.
- 5. Inductor 150 mH / 5A
- 6. C.R.O.
- 7. Patch cords.

PROCEDURE:

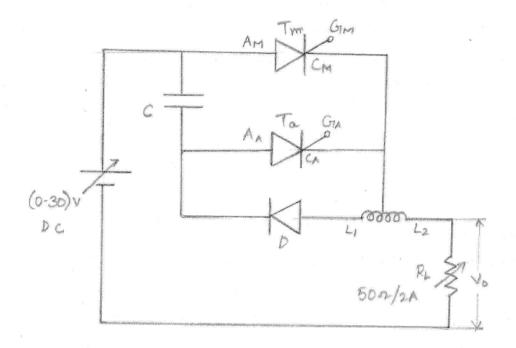
- 1. Make the connections as per the circuit diagram.
- 2. Switch on the Power Supplies of the main circuit and switching circuit.
- 3. Vary the firing angle in steps and record output voltage, thyristor voltage waveforms.
- 4. Note down the output voltage & output current from the voltmeter and ammeter.
- 5. Repeat the same procedure after connecting L load in series with the R load.

RESULT: The output of Single phase Single Phase fully controlled converter with R & RL loads is obtained and studied.

D. C. JONES CHOPPER

CIRCUIT DIAGRAM:

they.







5. DC JONES CHOPPER WITH R & RL LOADS

AIM: To obtain the output of DC Jones Chopper with R and RL Load. **THEORY:**

Chopper converts fixed DC Voltage to variable DC voltage. The control strategies used for control of DC DC choppers are Time Ratio Control and Current Limit Control.

Chopper circuit consists of a thyristor switch connected between the source and the load. The switch is closed & opened periodically such that the load is connected and disconnected from the supply alternatively. Thus the average voltage impressed on the load is controlled by controlling the ratio of ON state interval to one cycle duration.

The average output voltage of the chopper is given by

$$\mathbf{V}_{\text{avg}} = \left(\frac{T_{ON}}{T}\right) \mathbf{V}$$

Where V is input voltage, TON is ON time duration of the chopper. The ratio T_{ON}/T is called the duty ratio of the chopper. The duty ratio can be controlled in many ways such as by changing the ON period duty ratio by keeping frequency constant or by changing frequency and keeping ON period constant. Fixed frequency choppers with a variable ON period technique are generally used because of less harmonic contents.

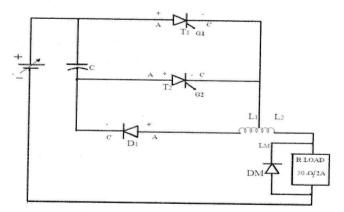


Fig 5.1: DC Jones Chopper

The Jones chopper circuit uses a Class-D commutation circuit. Here, an auxillary thyristor is used to turn OFF the main SCR TM. It is assumed that the capacitor C is initially charged to voltage with the polarity shown. When T_M is turned ON, the capacitor is discharged through it and through the inductor L. At the end of discharge cycle, the capacitor voltage will reverse and will be held by diode D to stay with this polarity when T_A is fired, the capacitor will discharge through TM and will turn it OFF. Since a reverse voltage is applied across the

TABULAR COLUMN :

Frequency : _____

| S.No. | Duty Ratio | Ton | Toff | Load Voltage (V) |
|--|------------|-----|------|------------------|
| in in the second se | | | | |
| | | | | |
| | s | | | |
| | | | | |

Duty Ratio : _____

in the second

| S.No. | Frequency (Hz) | Ton (ms) | Toff (ms) | Load Voltage (V) |
|--|-------------------|-------------|--------------|---------------------|
| | 2 | | N. 14. | |
| an a | | | | |
| | | | | |

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

•



TM immediately after turning ON the SCR, this phenomenon is known as Voltage Commutation.

APPARATUS:

- 1. Chopper power module
- 2. Chopper firing unit
- 3. Regulated Power supply (0-30)V
- 4. Loading Rheostat (50 Ω /2A)
- 5. Inductor -50 mH/2A
- 6. Multimeter.
- 7. CRO
- 8. Patch cords

PROCEDURE:

- 1. Make the connections as per the circuit diagram with R Load.
- 2. Keep the frequency knob and duty ratio knob at some intermediate position.
- 3. Set the DC power supply to 30V & switch ON the DC power supply to the chopper and the firing circuit.
- 4. Observe VO, VT1, VT2, VP1, VP2, VC waveforms on the CRO and note down the corresponding waveforms.
- 5. Keeping the frequency constant, vary the duty cycle in steps & note down T_{ON}, T_{OFF} and load voltage for each step.
- 6. Repeat the above step by varying frequency and keeping duty ratio constant.
- 7. Connect RL load and note down the output voltage VO & repeat the above procedure.

NOTE:

- 1. At lower frequencies, SCR may not turn ON due to insufficient voltage across the capacitor.
- 2. If the duty cycle is increased to large value, SCR may not turn OFF due to insufficient voltage across the capacitor to commutate the SCR. In such cases, switch OFF the kits and after some time switch ON and continue the procedure.

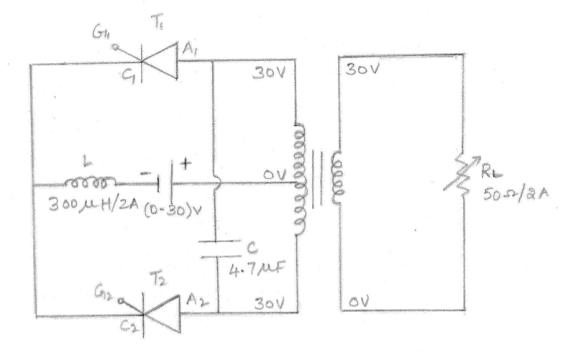
RESULT: The output of Single Phase Jones Chopper circuit and its operation is studied.

SINGLE PHASE PARALLEL INVERTER

CIRCUIT DIAGRAM:

Nin.

40





6. SINGLE PHASE PARALLEL INVERTER

AIM: To obtain the output of Single phase Parallel Inverter and study its operation with R & RL load.

THEORY:

An Inverter converts DC power into AC power at desired output voltage and frequency.

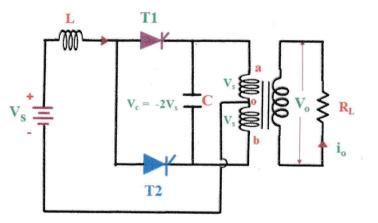


Fig 6.1 Parallel Inverter

In Single Phase Parallel Inverter, the capacitor is used for commutation of two thyristors $T_1 \& T_2$. An inductor is connected in series with the supply voltage because the source current becomes constant. During the operation of this inverter circuit, commutating capacitor C comes in parallel due to this, it is called Parallel Inverter.

In mode 1 operation, when SCR T_1 is fired, the current flows in the upper half of the primary winding. Here, SCR T_2 is OFF. This current produces magnetic flux which links with both the halves of the primary winding. Due to this, the capacitor charges to the voltage V_{DC} with upper plate positive w.r.t. lower plate.

In mode 2 operation, when SCR T_2 is triggered, the capacitor starts discharging with upper plate negative. Then T_1 gets into OFF state. Based on capacitor charging and discharging, the SCRs gets into OFF and ON states with positive and negative output voltages. When the capacitor current decays to zero, the capacitor voltage becomes $+2V_{DC}$. The same process is repeated for next cycle.

APPARATUS:

- 1. Parallel Inverter Module.
- 2. Regulated Power supply(0-30)V

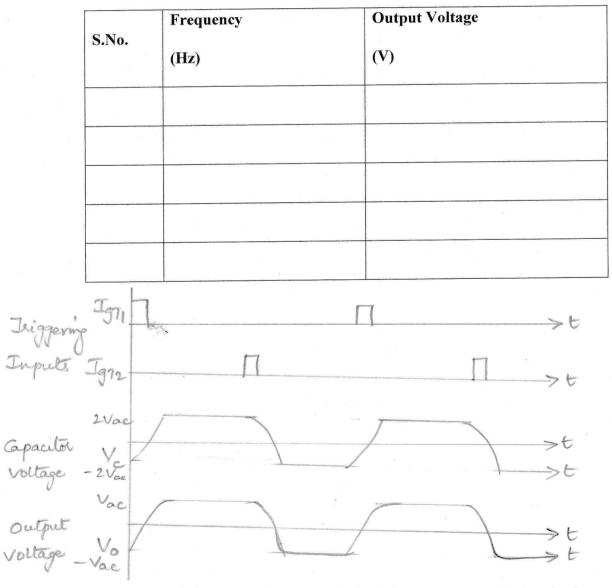
Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

TABULAR COLUMN:

R Load

| S.No. | Frequency (Hz) | Output Voltage (V) |
|-------|----------------|--------------------|
| | | |
| | | |
| | | |
| | | |
| | | |

RL Load



Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

- 3. Loading Rheostat $(50\Omega/2A)$
- 4. Inductor -50 mH/2A
- 5. Digital Multimeter.
- 6. Patch cords.
- 7. CRO.

PROCEDURE:

- 1. Make the connections as per the circuit diagram.
- 2. Adjust the DC supply to 15V and Switch ON the Main unit and the firing unit.
- 3. Set the frequency at a particular value and observe the load voltage waveform $V_0, V_{T1}, V_{T2}, V_{P1}, V_{P2}, V_C$ on CRO and note down the corresponding waveforms.
- 4. By changing the frequency, note down the output AC voltage using a multimeter.
- 5. Connect the RL load and repeat the same procedure

NOTE:

- 1. At lower frequencies SCR may not turn ON due to insufficient voltage across the capacitor. Hence adjust the frequency to a higher value (approximately above 100 Hz).
- 2. For commutation failure switch OFF the firing circuit as well as power circuit and switch it ON again.

RESULT: The output of Single Phase Parallel Inverter is observed and studied.



SINGLE PHASE CYCLO CONVERTER.

CIRCUIT DIAGRAM:

thing

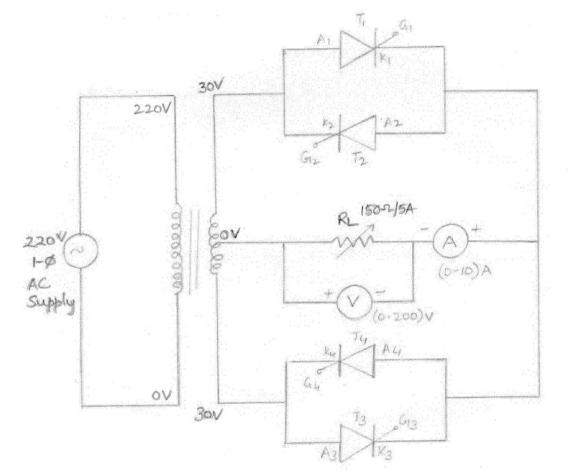


Fig 7.1

7.SINGLE PHASE CYCLO CONVERTER

AIM: To obtain the output of Single Phase Cyclo Converter circuit and to study its operation with R and RL loads.

THEORY:

Cyclo converter converts input power at one frequency to output power at a different frequency. Cyclo Converters are used in speed control of high power AC drives, induction heating etc.

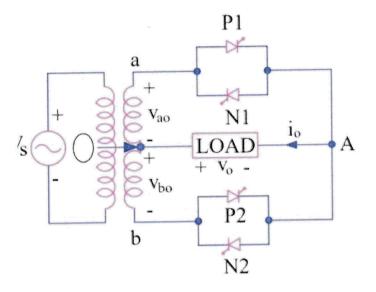


Fig 7.1: Single Phase Cyclo converter

The Single Phase Cycloconverter circuit is as shown above. The following sequence of operation can be followed One group of SCR's produces positive polarity load voltage and other group produces negative half cycle of the output. SCR's $P_1 \& N_2$ of the positive group are gated together depending on the polarity of the input. Only one of them is allowed conduct when a is positive with respect to O. SCR's $N_1 \& P_2$ of the negative group are gated together depending on the input. Only one of them is allowed together depending on the polarity of the input. Only one of the negative group are gated together with respect to O. SCR's $N_1 \& P_2$ of the negative group are gated together with respect to O. By triggering the respective SCR during negative or positive half cycles, any of the half cycle can be achieved at the load side. The order of switching sequence decides the frequency of Cyclo converter.

APPARATUS:

- 1. Cycloconverter Power unit.
- 2. Cycloconverter firing unit.

TABULAR COLUMN:

For R Load:

Vm = _____ Volts.

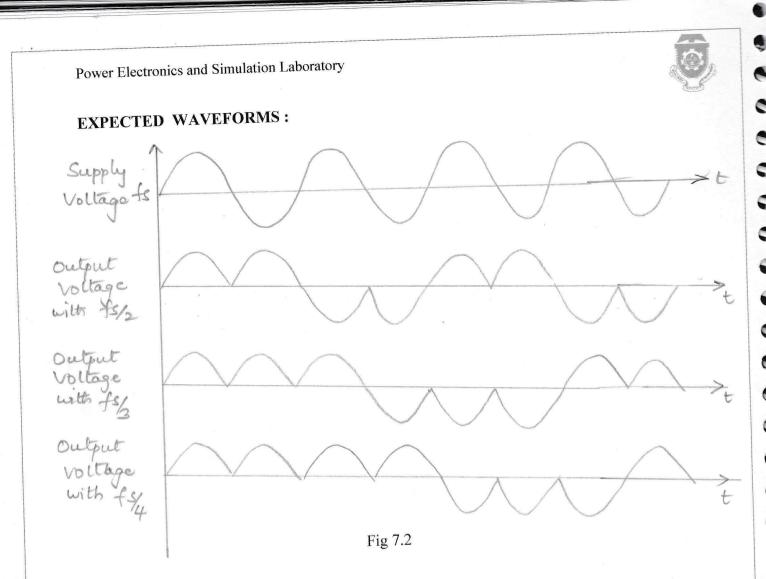
| S.No. | Frequency | VL (V) |
|-------|-----------|--------|
| - 1 | | |
| 2 | | |
| 3 | | |
| 4 | | |
| 5 | | 8 |
| 6 | | |
| 7 | | |

For RL Load :

Vm = _____ Volts.

| S.No. | Frequency | V _L (V) |
|-------|----------------------------|---|
| 1 | | |
| 2 | | |
| 3 | | × |
| 4 | | • |
| 5 | | |
| 6 | | |
| 7 | | |
| | 1 2 3 4 5 6 | 1 2 3 4 5 6 |

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology



.

iting.

- 3. Single Phase Isolation transformer (center tapped)
- 4. Loading Rheostat $150\Omega/2A$
- 5. Inductor -(0-150 mH / 5A)
- 6. Digital Multimeter.
- 7. C.R.O.
- 8. Patch cards.

PROCEDURE:

- 1. Make the connections as per the circuit diagram.
- 2. Switch ON the power unit and the firing unit .
- 3. Set the frequency division to 2., note down the waveform across the load Vo and note down the output voltage and current readings from the voltmeter and the ammeter.
- 4. Note down the output voltage waveform for different frequency divisions and note down the output voltages and currents.
- 5. Now connect RL load.
- 6. Repeat the above steps for Cyclo Converter with RL load.

RESULT: The output and operation of Single Phase Cycloconverter with R & RL load is observed.

SINGLE PHASE SERIES INVERTER

CIRCUIT DIAGRAM :

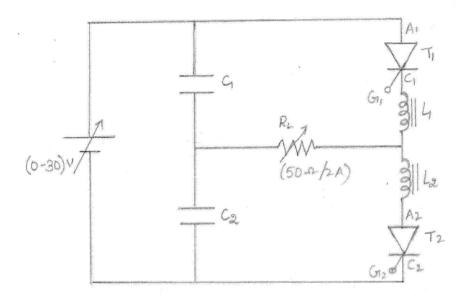


Fig 8.1

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

•

8. SINGLE PHASE SERIES INVERTER

AIM: To obtain the output of Single phase Series Inverter circuit with R and RL Load and study its operation.

THEORY:

In Series Inverter, commutating components are permanently connected in series with the load. Series Inverters are also classified as self-commutated inverters & Load commutated Inverters.

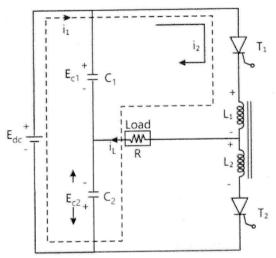


Fig 8.1: Series Inverter

This circuit consists of load resistance R in series with commutating components L & C. The values of L & C are so chosen that the series RLC circuit forms an under damped circuit. Two thyristors T1 and T2 are turned on appropriately so that output voltage of desired frequency can be obtained.

When thyristor T1 is turned ON with T2 OFF, current starts building up in the RLC circuit. As the circuit is under damped, the load current after reaching peak value, decays to zero. After thyristor T1 has commuted, upper plate of capacitor attains positive polarity. Now, when T2 is turned ON, capacitor discharges and load current flows in reverse direction up to some peak negative value and then decays to zero. The capacitor sores charge during one half cycle and releases the same amount of charge during next half cycle.

APPARATUS:

- 1. Series Inverter unit
- 2. Loading Rheostat $50\Omega/2A$
- 3. Regulated Power supply (0-30)V

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

TABULAR COLUMN:

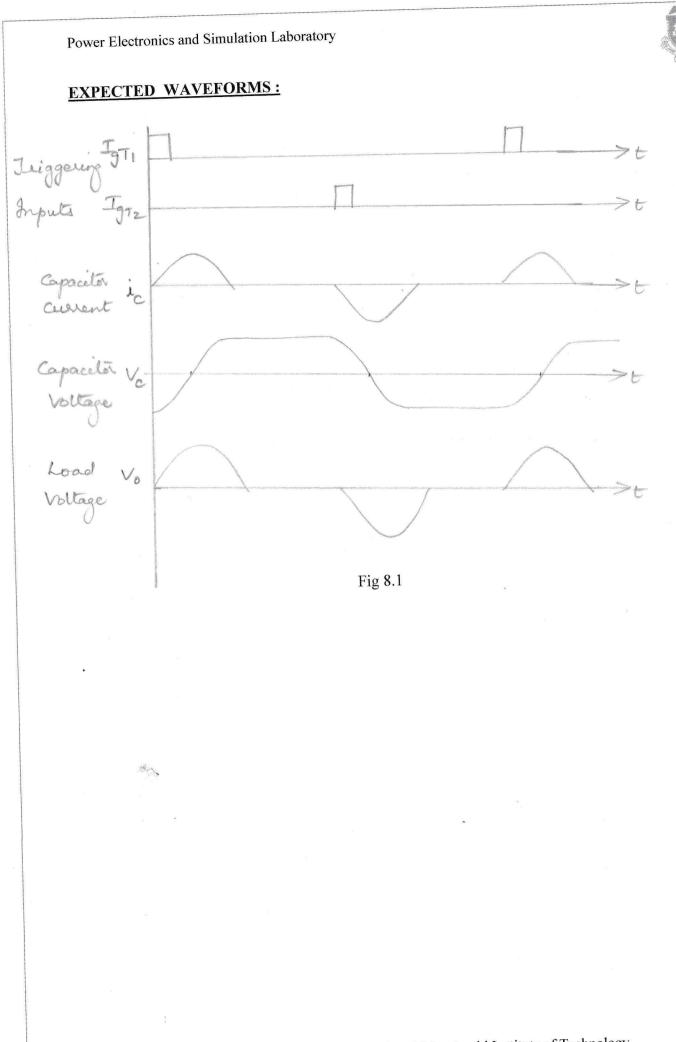
R Load

| aNO | | Time Period | Frequency | Output voltage | |
|--|---------|-------------|-----------|----------------|--|
| S.NO. | | (ms) | (Hz) | | |
| | | | | | |
| | * ** | | | | |
| an a | | | | | |
| | 6. | | | | |
| | | | - | | |
| | | | | | |

RL Load

| C NO | Time Period | Frequency | Output voltage |
|-------|-------------|-----------|----------------|
| S.NO. | (ms) | (Hz) | (V) |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology



Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

Į,

- 4. Inductor -50 mH / 2A
- 5. Multimeter.
- 6. Patch cords

it in

7. CRO

PROCEDURE:

- 1. Make the connections as per the circuit diagram with R Load.
- 2. Adjust the DC supply voltage to 30 V and Switch ON the DC power supply and the firing unit.
- 3. Set the frequency at a particular position and observe the output waveform V_0, V_{T1} , $V_{T2}, V_{P1}, V_{P2}, V_{C1}, V_{C2}$ on the CRO and note down the corresponding waveforms.
- 4. By varying the frequency in steps, note down the AC output voltage using multimeter.
- 5. Connect RL load and note down the output voltage V_0 and repeat the same procedure. **NOTE:** In case of Commutation failure, switch OFF the power module and the firing unit and again switch it ON.

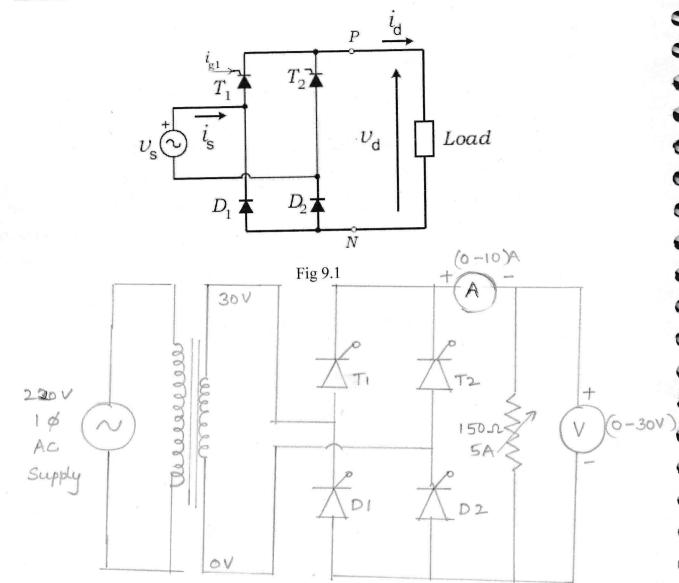
RESULT: The output of Single Phase Series Inverter and its operation with R& RL load is observed and studied.

SINGLE PHASE HALF CONTROLLED CONVERTER

CIRCUIT DIAGRAM:

dia.

ju.t.



Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology



9. SINGLE PHASE HALF CONTROLLED CONVERTER

AIM: To obtain the output of Single phase Half Controlled Bridge Converter and study the operation.

THEORY:

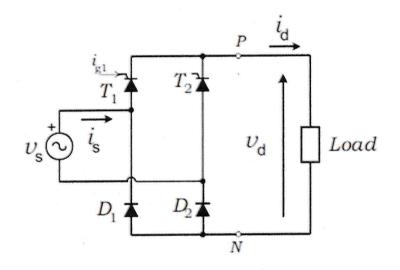


Fig 9.1: Single Phase Half controlled Converter

The Single Phase Half controlled Converter circuit consists of two SCR's and two diodes. During the positive half cycle, the SCR T₁ and diode D₂ conduct when triggered at firing angle α . T₁ and D₂ conducts from α to π . For negative Half cycle, the SCR T₂ and diode D₁ conducts from $\pi + \alpha$ to 2 π .

This converter will not allow negative voltage across the load as it turns off soon after the diode gets reverse biased. It has better power factor due to this reason and is commonly used in application up to 15KWatts and it has lot of advantages compare to fully controlled converter like low cost, good power factor and low load current ripple. Some of the disadvantages are higher harmonic content in the source current and since the output voltage cannot be made negative, inverter operation is not possible.

APPARATUS:

- 1. Single phase Half controlled Bridge Converter power circuit.
- 2. Single phase Converter firing circuit.
- 3. Single phase Isolation transformer 230V/2A
- 4. R Load 50 ohms / 2Amps.

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

TABULAR COLUMN:

| Input Voltage (Vin) | | Firing angle(α) | Output voltage(V) | Output Current |
|---------------------|---------------------|---------------------|-------------------|---------------------------------|
| | | | 2 | |
| | 1 | | | |
| × | | | | |
| | | | x | |
| | 1 | | | |
| | 1 | | | |
| | | | | |
| | <u> </u> | | | |
| | Input Voltage (Vin) | Input Voltage (Vin) | angle(a) | Input voltage (vm) angle(α) |

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology



- 5. L Load
- 6. CRO

PROCEDURE:

- 1. Switch ON the Mains Supply to the Firing circuit. Observe all the test points by varying the firing angle and trigger outputs ON/OFF switch.
- 2. Switch ON the main circuit supply and firing circuit and note down the voltage wave forms across load and devices for firing angle zero.
- 3. Note down the wave forms across load and devices for different firing angles.
- 4. Repeat the same procedure for different firing angles.
- 5. Repeat the same for R-L load with and without freewheeling diode and note down the wave forms.

RESULT : The operation of single phase Half controlled converter and wave forms for different firing angles are observed.



CIRCUIT DIAGRAM:

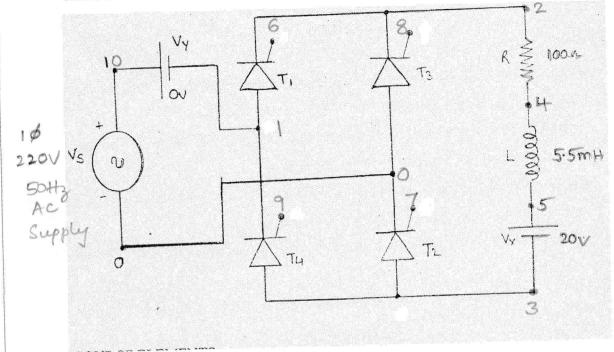
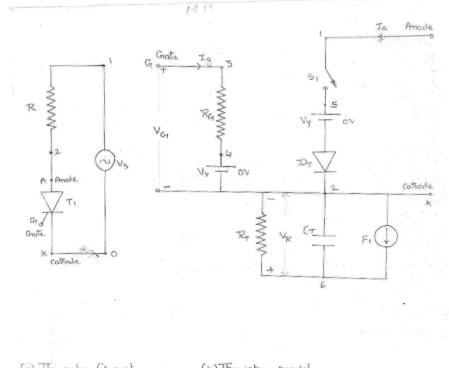


Fig 10.1



(a) Thyristor Escuit (b) Thyristor model





.

10. SIMULATION OF SINGLE-PHASE FULL CONVERTER USING RLE LOADS AND SINGLE-PHASE AC VOLTAGE CONTROLLER USING RLE LOADS.

a) SINGLE PHASE FULL CONVERTER USING RL AND E LOAD

AIM: To simulate single phase full converter using PSPICE and obtain its output.

APPARATUS: Computer and PSPICE Software

THEORY:

PSpice A/D is a simulation program that models the behaviour of a circuit containing any mix of analog and digital devices. Because the analog and digital simulation algorithms are built into the same program, PSpice A/D simulates mixed-signal circuits with no performance degradation because of tightly coupled feedback loops between the analog and digital sections.

PSpice A/D can perform DC, AC, and transient analyses, so the response of a circuit to different inputs can be tested. The range of models built into PSpice A/D include resistors, inductors, capacitors, and bipolar transistors, diodes and different types of sources.

.TRAN (transient analysis)

Purpose: The .TRAN command causes a transient analysis to be performed on the circuit and specifies the time period for the analysis.

General form .TRAN[/OP] +[no-print value [step ceiling value]][SKIPBP]

Examples .TRAN 1ns 100ns

.TRAN/OP 1ns 100ns 20ns SKIPBP

.TRAN 1ns 100ns 0ns .1ns

.TRAN 1ns 100ns 0ns {SCHEDULE(0,1ns,25ns,.1ns)}

.PROBE (Probe)

Purpose: The .PROBE command writes the results from DC, AC, and transient analyses to a data file used by Probe.

General form .PROBE[/CSDF][output variable]

Examples .PROBE .PROBE V(3) V(2,3) V(R1) I(VIN) I(R2) IB(Q13) VBE(Q13)

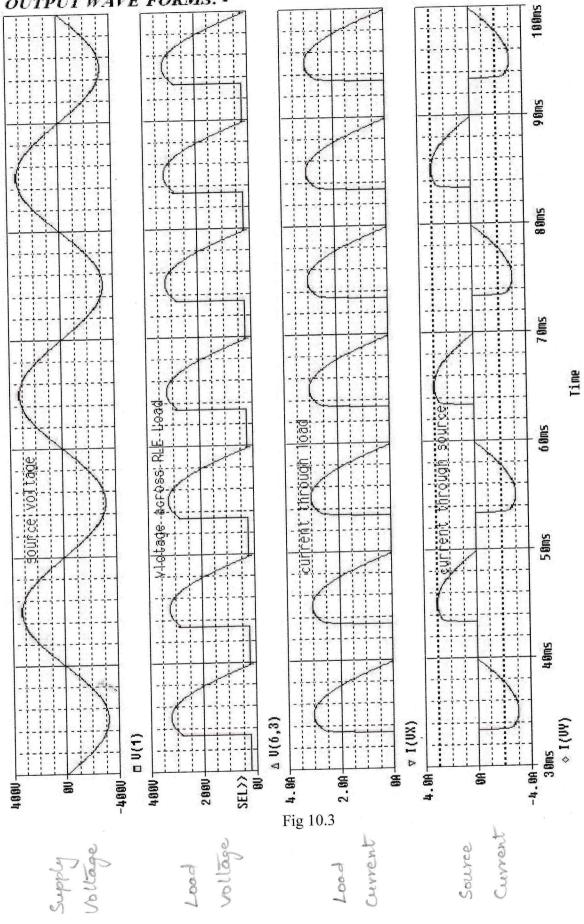
OPTIONS (analysis options)

Purpose: The .OPTIONS command is used to set all the options, limits, and control parameters for the simulator.

General form .OPTIONS [option name]* [<option name>= <value>]*







Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

×



FOURIER COMPONENTS OF TRANSIENT RESPONSE I(VY) DC COMPONENT = -2.420296E-07

HARMONIC FREQUENCY FOURIER NORMALIZED NORMALIZED PHASE PHASE (DEG) COMPONENT COMPONENT (DEG) NO (HZ) 1.000E+00 -1.632E+01 0.000E+00 2.495E+00 5.000E+01 1 1.801E+02 1.474E+02 2.025E-07 2 1.000E+02 5.052E-07 1.963E+02 1.474E+02 3.092E-01 7.715E-01 3 1.500E+02 9.656E+01 3.130E+01 1.892E-07 4.720E-07 4 2.000E+02 1.398E+02 5.824E+01 1.610E-01 5 2.500E+02 4.018E-01 2.072E+00 -9.582E+01 2.158E-07 5.385E-07 6 3.000E+02 7.917E-02 -7.201E+01 4.220E+01 1.976E-01 3.500E+02 7 2.774E+02 1.469E+02 1.735E-07 4.328E-07 8 4.000E+02 1.616E+02 3.085E+02 8.054E-02 2.010E-01 9 4.500E+02

TOTAL HARMONIC DISTORTION = 3.664522E+01 PERCENT JOB CONCLUDED TOTAL JOB TIME .27 Sec

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

OUTPUT: *******Diode MODEL ****** *** XT4.DMOD XT3.DMOD XT2.DMOD XT1.DMOD 2.200000E-15 2.200000E-15 2.200000E-15 2.200000E-15 IS 1.200000E+03 1.200000E+03 1.200000E+03 1.200000E+03 BV MODEL Switch *******Voltage Controlled **** ********** XT2.SMOD XT4.SMOD XT1.SMOD XT3.SMOD .0105 .0105 .0105 RON .0105 1.000000E+06 1.000000E+06 1.000000E+06 1.000000E+06 ROFF .5 .5 .5 .5 VON 0 0 VOFF 0 0 TEMPERATURE = 27.000 DEG C ********INITIAL TRANSIENT SOLUTION ***** *** NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE 1) 0.0000 (2) 10.0000 (3) -9.9998 (4) 10.0000 5) 10.0000 (6) 10.0000 (7) 0.0000 (8) 10.0000 9) 0.0000 (10) 0.0000 (XT1.4) 10.0000 (XT1.5) 10.00E-06 (XT1.6) 10.0000 (XT1.7) 10.00E-06 (XT2.4) 0.0000 (XT2.5) -9.9998 (XT2.6)-110.0E-12 (XT2.7) -9.9998 (XT3.4) 10.0000 (XT3.5) 10.00E-06 (XT3.6) 10.0000 (XT3.7) 10.00E-06 (XT4.4) 0.0000 (XT4.5) -9.9998 (XT4.6)-110.0E-12 (XT4.7) -9.9998 VOLTAGE SOURCE CURRENTS CURRENT NAME VS 4.163E-16 VG1 0.000E+00 VG2 0.000E+00 VG3 0.000E+00 VG4 0.000E+00 VX -2.000E-11 VY -4.163E-16 XT1.VX 0.000E+00 -1.000E-11 XT1.VY XT2.VX 0.000E+00 XT2.VY -1.000E-11 XT3.VX 0.000E+00XT3.VY -1.000E-11 XT4.VX 0.000E+00 XT4.VY -1.000E-11 TOTAL POWER DISSIPATION 4.00E-10 WATTS TEMPERATURE = 27.000 DEG C *******FOURIER ANALYSIS *****

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology



PROCEDURE:

1. Write the Program in PSPICE .cir file or in .txt file, by identifying nodes in the circuit.

2. Save the program and run it in PSPICE A/D.

3. Observe the Output file for outputs like nodal voltages, source currents and power dissipated.

4. Open probe and enter the waveforms to be plotted and get the plots.

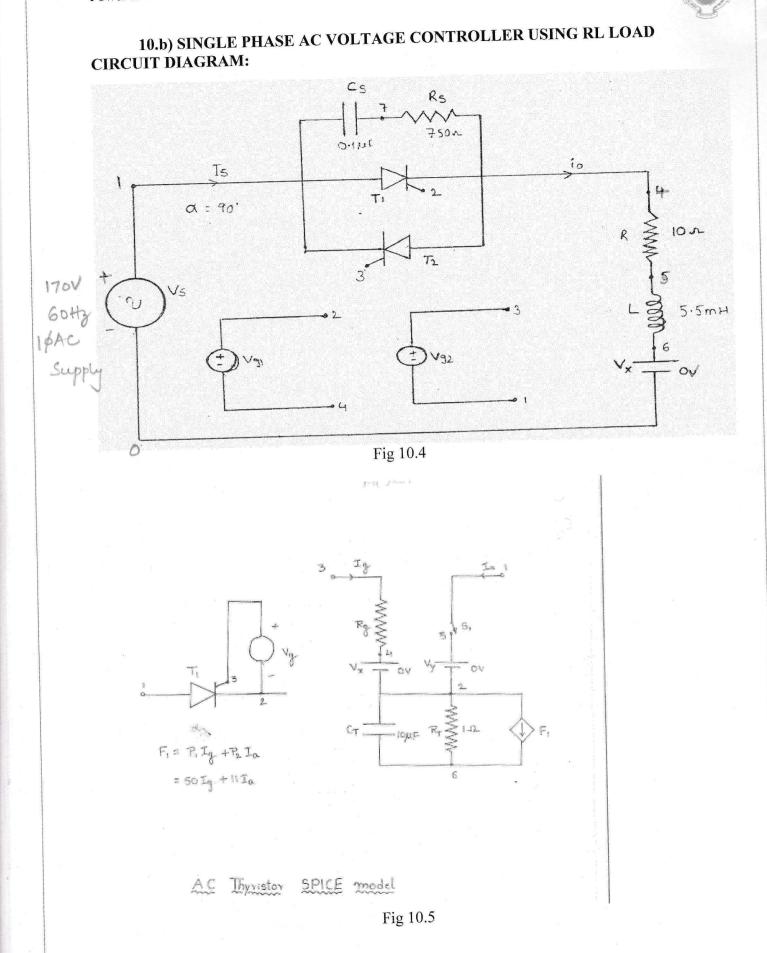
5. Note down the plots in graph sheets and verify it with theoretical values.

PROGRAM:

********SINGLE PHASE AC SUPPLY********* VS 10 0 SIN(0 325V 50HZ) VG1 6 2 PULSE(0V 10V 3333.33US 1NS 1NS 100US 20000US) VG2 7 0 PULSE(0V 10V 3333.33US 1NS 1NS 100US 20000US) VG3 8 2 PULSE(0 10V 13333.33US 1NS 1NS 100US 20000US) VG4 9 1 PULSE(0 10V 13333.33US 1NS 1NS 100US 20000US) R 2 4 1000HM L 4 5 5.5MH VX 5 3 DC 20V VY 10 1 DC 0V XT1 1 2 6 2 SCR XT2 3 0 7 0 SCR XT3 0 2 8 2 SCR XT43191SCR ****************************Begin of Sub circuit for SCR************************* .SUBCKT SCR 1 2 3 2 S11562SMOD RG 3 4 50 VX 4 2 DC 0V VY 57 DC 0V DT 7 2 DMOD RT 6 2 1 CT 6 2 10UF F1 2 6 POLY(2) VX VY 0 50 11 .MODEL SMOD VSWITCH (RON=0.0105 ROFF=10E+5 VON=0.5V VOFF=0V) .MODEL DMOD D(IS=2.2E-15 BV=1200V TT=0 CJO=0) .ENDS SCR TRAN 50US 100MS 30MS 50US .OPTIONS ABSTOL=1.00N RELTOL=1.0M VNTOL=0.01 ITL5=20000 .FOUR 50HZ I(VY) .PROBE .END

RESULT: The response of single phase full wave bridge converter is verified using SPICE software.

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology



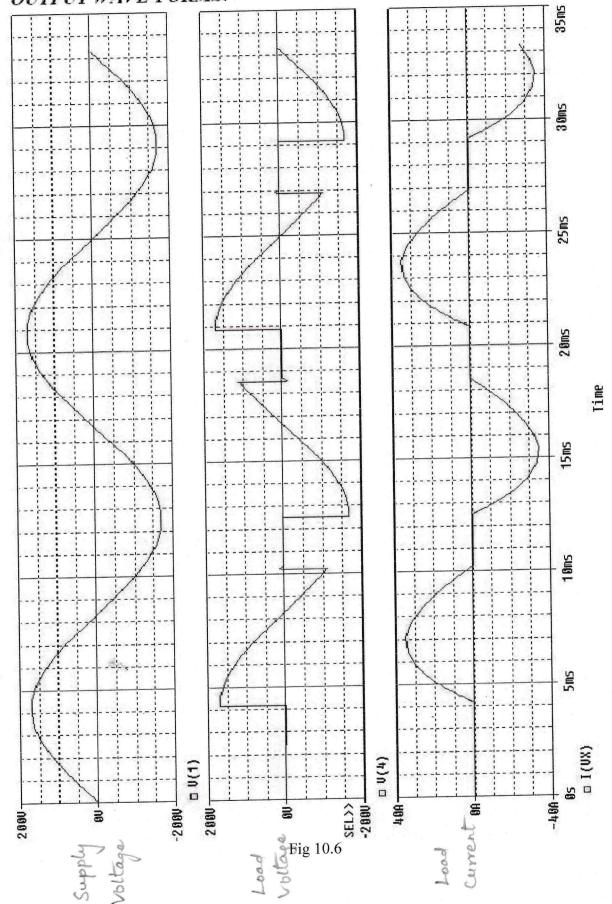
Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

.

4.2



OUTPUT WAVE FORMS: -



Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

.

OUTPUT:

| OUIPUI. | | | |
|---|-----------------------------|-------------------------|------------|
| ********VOLTAGE | CONTROLLED | SWITCH | MODEL |
| PARAMETERS*********** | *** | **** | ***** |
| PARAMETERS*********************************** | **** | | |
| * * * | | | |
| XT1.SMOD XT2. | SMOD | | |
| RON 01 .01 | | | |
| ROFF 1.000000E+06 1 | .000000E+06 | | |
| VON .1 .1 | | | |
| VOFF 0 0 | | PERATURE = 27.0 | 00 DEG C |
| ********INITIAL TRANSIEN | T SOLUTION IEM | PEKATURE = 27.0 | **** |
| *******INITIAL TRANSIEN ****** | **** | | |
| *** | | VOLTAGE NOD | F VOLTAGE |
| *** NODE VOLTAGE NODE | VOLTAGE NODE | 0.0000 | L TOLLE |
| (1) 00000 (2) 00000 | (3) 0.0000 (4) | 0.0000 | |
| (5) 0.0000 (6) 0.0000 | $() 0.0000 (\Lambda 11.4)$ | 0.0000 | |
| VOLTAGE SOURCE CURF | RENTS | | |
| NAME CURRENT | | | |
| VS 0.000E+00 | | | |
| VG1 0.000E+00 | | | |
| VG2 0.000E+00 | | | |
| VX 0.000E+00 | | | |
| XT1.VX 0.000E+00 | | | |
| XT1.VY 0.000E+00 TOTAL POWER DISSIP. | ATION 0.00E+00 WA | TTS | |
| | | | DEG C |
| *********FOURIER ANALY ********* | **** | ***** | **** |
| | | | |
| *** FOURIER COMPONENTS O | F TRANSIENT RESPO | NSE V(4) | |
| | | | |
| THE FREQUENCY | TOURIER NORMA | LIZED PHASE | NORMALIZED |
| TTO (TTO) COMPON | HALLUNPUNDINI | | (DEG)P |
| 101101 | 02 1.000E+00 -1.788E | $\pm 01 0.000E \pm 00$ | |
| | 4 9.459E-06 -8.191E | +01 - 4.614E + 01 | |
| 2 1.200E+02 9.565E-0 3 1.800E+02 6.167E+0 |)1 6.098E-01 6.883E | +01 1.225E+02 | |
| 4 2.400E+02 9.083E-0 | 4 8.982E-06 -6.561E | | |
| 5 3.000E+02 3.372E+0 |)1 3.335E-01 -6.876E | | |
| 6 3.600E+02 9.699E-0 | 4 9.591E-06 -5.180E | | |
| 7 4.200E+02 7.505E+0 | 00 7.421E-02 1.232E | | |
| 8 4.800E+02 1.003E-0 | | | |
| a 5 100E 102 1 208E+ | 01 1.293E-01 -1.270H | | |
| TOTAL HARMONIC DIS | TORTION = 7.108297 | ETVI PERCENT | |
| JOB CONCLUDED | | | |
| TOTAL JOB TIME | .05 sec | | |

0

.

6

•

.

C

C

¢

•

6

C

0

C

.

5

đ

(

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

•



.OPTIONS ABSTOL=1.00n RELTOL=1.0m VNTOL=1.0m ITL5=10000

.FOUR 60HZ V(4)

.END

RESULT: The response of single phase AC voltage controller is verified using SPICE software.

SIMULATION OF RESONANT PULSE COMMUTATION CIRCUIT

CIRCUIT DIAGRAM:

Bir.

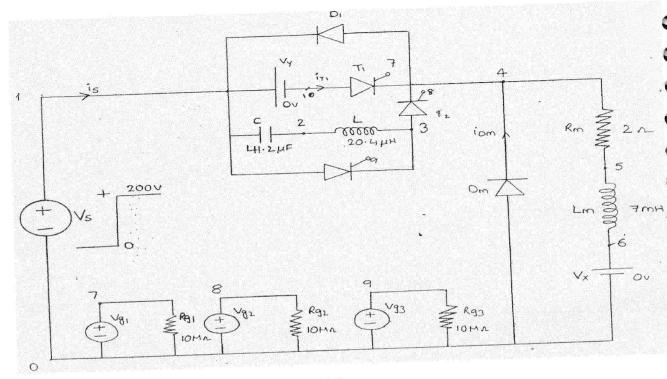


Fig 11.1

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

•



11. SIMULATION OF RESONANT PULSE COMMUTATION CIRCUIT

AIM: To simulate Resonant commutation using PSPICE and obtain its output.

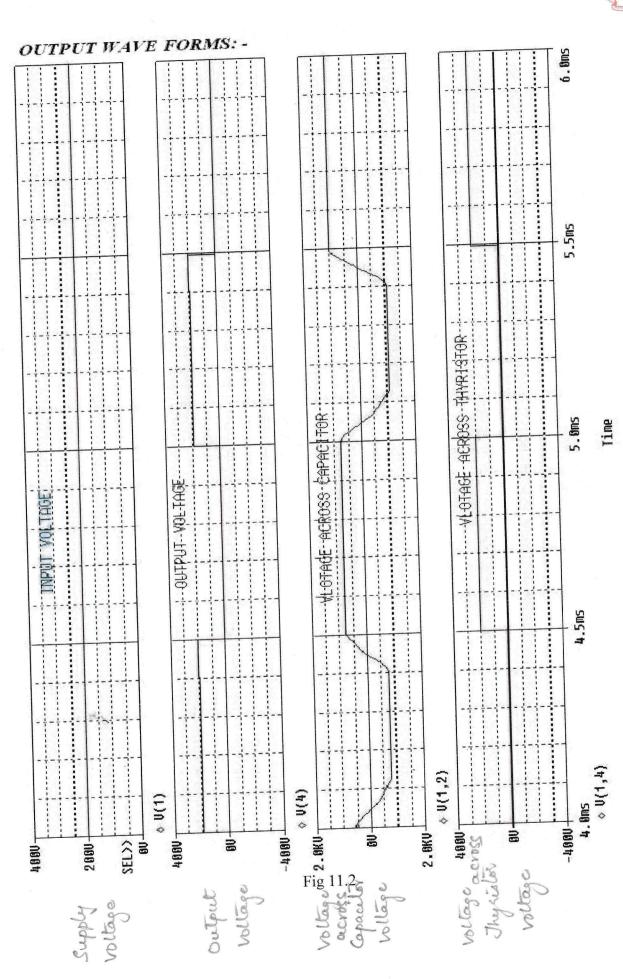
APPARATUS: Computer and PSPICE software

PROCEDURE:

- 1. Write the Program in PSPICE .cir file or in .txt file, by identifying nodes in the circuit.
- 2. Save the program and run it in PSPICE A/D.
- 3. Observe the Output file for outputs like nodal voltages, source currents and power dissipated.
- 4. Open probe and enter the waveforms to be plotted and get the plots.
- 5. Note down the plots in graph sheets and verify it with theoretical values.

PROGRAM:

************SINGLE PHASE AC SUPPLY***** VS 1 0 DC 200V 1US 1US 0.4MS 1MS) VG1 7 0 PULSE(0V 100V 0 VG2 8 0 PULSE(0V 100V 0.4MS 1US 1US 0.6MS 1MS) 1US 1US 0.2MS 1MS) VG3 9 0 PULSE(0V 100V 0 **********LOAD*************** RG17010MEG RG2 8 0 10MEG RG3 9 0 10MEG L 2 3 20.4UH C 1 2 41.2UF IC=200V D1 4 1 DMOD DM 0 4 DMOD .MODEL DMOD D(IS=1E-25 BV=1000V) RM 452 LM 5 6 7MH VX 6 0 DC 0V VY 1 10 DC 0V *****SWITCHES**** XT1 10 4 7 0 TMOD XT2 3 4 8 0 TMOD XT31 390 TMOD *****************************Begin of Sub circuit for SCR***** .SUBCKT TMOD 1 2 3 4 DT 5 2 DMOD ST 1 5 3 4 SMOD .MODEL DMOD D(IS=2.22E-15 BV=1200V CJO=0 TT=0) .MODEL SMOD VSWITCH (RON=0.01 ROFF=10E+6 VON=10V VOFF=5V) .ENDS TMOD *********************************End of Sub circuit for SCR********* .PROBE TRAN 1US 6MS 4MS



Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

.

Power Electronics and Simulation Laboratory



| OUTPUT: | MODEL |
|---|--------------------|
| *****DIODE PARAMETERS*********************************** | |
| PARAMETERS*********************************** | ***** |
| | |
| *** DMOD XT1 DMOD XT2.DMOD XT3.DMOD | |
| DMOD ATT.DMOD ATZ.DMOD 15 2220000E 15 | |
| IS 100.00000E-27 2.220000E-10 2.220000E+02 1.200000E+02 | |
| BV 1.000000E+03 1.200000E+03 1.200000E+03 1.200000E+03 | |
| **********Voltage Controlled Switch | MODEL |
| ************* VAITAGE CONTONICO | |
| PARAMETERS*********************************** | |
| ATT.SWOD ATE.STOC | |
| | |
| ROFF 10.000000E+06 10.000000E+06 10.000000E+06 | |
| VON 10 10 10 | |
| VOFF 5 5 5 | |
| ********INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 | 0 DEG C ******* |
| *** | VOLTAGE |
| NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE | VOLINOL |
| (1) 200.0000 (2) 39.88E-09 (3) 39.88E-09 (4) 39.88E-06 | |
| (5) 0,0000 (6) 0,0000 (7) 0,0000 (8) 0,0000 | |
| (9) 0.0000 (10) 200.0000 (XT1.5) .5928 (XT2.5) 40.31E-09 | |
| (XT3.5) .5928 | |
| | |
| VOLTAGE SOURCE CURRENTS | |
| NAME CURRENT | |
| | |
| VS -1.994E-05 | |
| VG1 0.000E+00 | |
| | |

VG2 0.000E+00 VG3 0.000E+00 VX 1.994E-05 VY 1.994E-05

TOTAL POWER DISSIPATION 3.99E-03 WATTS

JOB CONCLUDED

TOTAL JOB TIME .08 Sec

Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

.

Rich

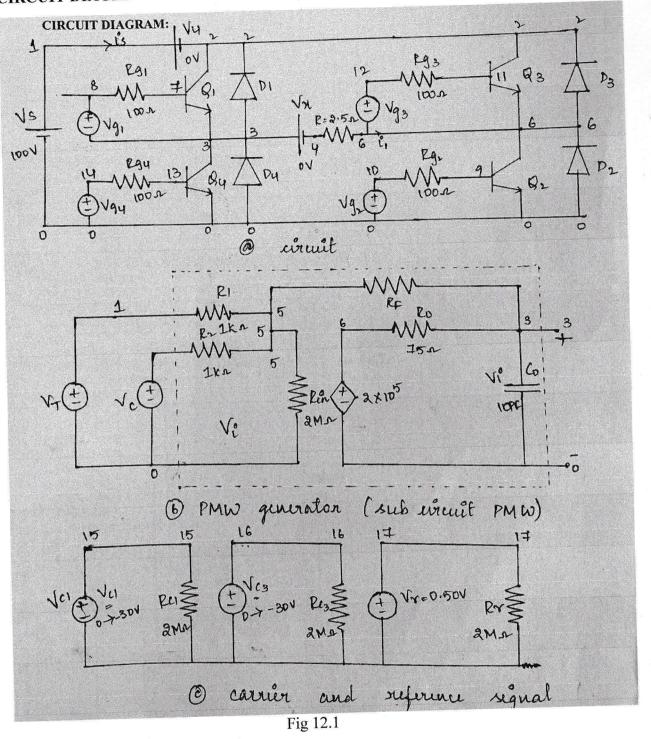


.OPTIONS ABSTOL=1.000U RELTOL=0.01 VNTOL=0.1 ITL5=20000 .END

RESULT: The response of Resonant commutation circuit is verified using SPICE software.

.

SIMULATION OF SINGLE PHASE INVERTER WITH PWM CONTROL. CIRCUIT DIAGRAM:



Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

•



12. SIMULATION OF SINGLE PHASE INVERTER WITH PWM CONTROL.

AIM: To simulate single phase inverter with PWM controller using PSPICE and obtain its output.

APPARATUS: Computer and PSPICE software

PROCEDURE:

- 1. Write the Program in PSPICE .cir file or in .txt file, by identifying nodes in the circuit.
- 2. Save the program and run it in PSPICE A/D.
- 3. Observe the Output file for outputs like nodal voltages, source currents and power dissipated.
- 4. Open probe and enter the waveforms to be plotted and get the plots.
- 5. Note down the plots in graph sheets and verify it with theoretical values.

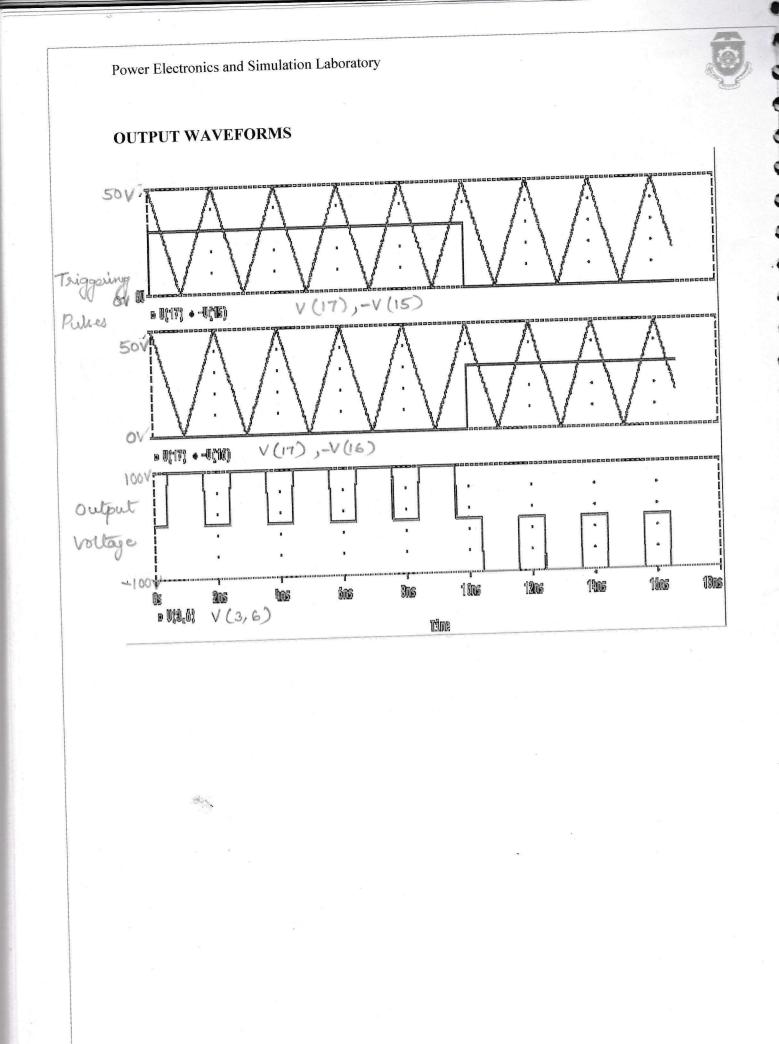
PROGRAM:

**** CIRCUIT DESCRIPTION : 1-PH PWM INVERTER

VS 1 0 DC 100V VR 17 0 PULSE(50V 0V 0 1MS 1MS 1NS 2MS) **RR 17 0 2MEG** VC1 15 0 PULSE(0 -30V 0 1NS 1NS 10MS 20MS) RC1 15 0 2MEG VC3 16 0 PULSE(0 -30V 10MS 1NS 1NS 10MS 20MS) RC3 16 0 2MEG R 4 6 2.50HM VX 3 4 DC 0V VY 1 2 DC 0V D1 3 2 DMOD D2 0 6 DMOD D3 6 2 DMOD D4 0 3 DMOD .MODEL DMOD D(IS=2.2E-15 BV=1890V) Q1 2 7 3 QMOD Q2 6 9 0 QMOD O3 2 11 6 QMOD Q4 3 13 0 QMOD .MODEL QMOD NPN(IS=6.73F BF=416.4 CJC=3.638P CJE=4.493P) RG1 8 7 1000HM RG2 10 9 1000HM RG3 12 11 1000HM RG4 14 13 1000HM

XPW1 17 15 8 3 PWM XPW2 17 15 10 0 PWM XPW3 17 16 12 6 PWM XPW4 17 16 14 0 PWM

.SUBCKT PWM 1 2 3 4 R1 1 5 1K R2 2 5 1K



Department of Electrical and Electronics Engineering, Vidya Jyothi Institute of Technology

in an



RIN 2 0 2MEG R0 6 3 75OHM C0 3 4 10PF RF 5 3 100K E1 6 4 0 5 2E+5 .ENDS PWM .TRAN 10US 16.67MS 0 10US .OPTIONS ABSTOL=1.00N RELTOL=0.01 VNTOL=0.1 ITL5=20000 .PROBE .END

RESULT: The output voltage and currents of PWM Inverter are observed by simulating the circuit in PSPICE.

Vidya Jyothi Inst@ute of Technology (A Autonomous Institution)



(Accredited by NAAC, Approved by AICTE New Delhi & Permanently Affiliated to JNTUH)

Aziznagar Gate, C.B. Post, Hyderabad-500 075

Artment of Electrical and Electronics Engineering (Accredited by NBA)

LAB ASSESSMENT

2020-21

Name of the Laboratory: Power

| | Electronic | s & 8 | Simula | ation | | Bran | ch/Sec | ction: | Α | | | | | Year | /Sem: | III-II | [| | Page: | | |
|-----|------------|-------|--------|-------|----|------|--------|--------|-------|-------|-------|----|----|------|-------|--------|----|--------|--------|--------|------|
| | | | | | | | | Day t | o Day | Asses | sment | | | | | | | Day To | Record | Intern | |
| S.N | Roll | | | | | | | | Ŵ | eek | | _ | | | | , | | Day | (5) | al | Mark |
| 05. | Number | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | | | | |
| 1 | 18911A0201 | S | 9 | 9 | 9 | 9 | 10 | 10 | 10 | 10 | 10 | | | | | | | 10 | 5 | 8 | 23 |
| 2 | 18911A0202 | 9 | 9 | 9 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | | | | | | | 10 | 5 | 8 | 23 |
| 3 | 18911A0203 | 8 | 8 | 8 | 8 | 9 | 9 | 9 | 9 | 9 | 9 | | | | 6 | | | 9 | 5 | 7 | 21 |
| 4 | 18911A0204 | 7 | 7 | 7 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | | | | | | | 8 | 5 | AB | 13 |
| 5 | 18911A0205 | 7 | 17 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | | | | | | | 8 | 5 | 7 | 20 |
| 6 | 18911A0206 | 8 | 8 | 8 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | | | | | | | 9 | 5 | 7 | 21 |
| 7 | 18911A0208 | 9 | 9 | 9 | 10 | 10 | 10 | 10 | 10 | 9 | 10 | | | | | | | 10 | 5 | 8 | 23 |
| 8 | 18911A0209 | 8 | 8 | 8 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | | | | | | | 9 | 5 | 8 | 22 |
| 9 | 18911A0210 | 8 | 8 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | | | | | | | 9 | 5 | 7 | 21 |
| 10 | 18911A0211 | 9 | 9 | 9 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | | | _ | | | | 10 | 5 | 8 | 23 |
| 11 | 18911A0212 | 8 | 8 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | | | | | | | 9 | 5 | 9 | 23 |
| 12 | 18911A0213 | 8 | 8 | 8 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | | | | | | | 9 | 5 | 7 | 21 |
| 13 | 18911A0214 | 8 | 8 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | | | | | | | 9 | 5 | 8 | 22 |
| 14 | 18911A0215 | 7 | 7 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | | | | | | | 8. | 5 | 10 | 23 |
| 15 | 18911A0216 | 8 | 8 | 9 | 9 | 9 | 9 | q | 9 | 9 | 9 | | | | | | | 9 | 5 | 7 | 21 |
| 16 | 18911A0218 | 9 | 9 | 9 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | | | | | | | 10 | 5 | 8 | 23 |
| | 18911A0219 | 8 | 8 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | | | | | | | 9 | 5 | - | 2 |
| | 18911A0220 | 8 | 8 | 9 | g | 9 | 9 | 9 | 9 | 9 | 9 | | | | | | | 9 | 5 | 8 | 22 |
| | 18911A0221 | -1 | 7 | 8 | È | 8 | 8 | 8 | 8 | 8 | 8 | | | | | | | 8 | S | 🦸 🧍 | 22 |
| | 18911A0223 | 8 | 8 | 8 | 9 | 9 | 9 | 9. | 9 | 9 | 9 | | | | | | | 9 | 5 | 7 | 21 |
| | 18911A0224 | 6 | 6 | 7 | 7 | 7 | 7 | 1 | 7 | 7 | 7 | | | | | | | 7102 | 5 | 8 | 20 |
| | 18911A0225 | 8 | 8 | 8 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | | | | | | | 9 | 5 | 7 | 21 |
| | 18911A0226 | 7 | 7 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | | | | | | | 8 | 5 | 6 | 19 |
| | 8911A0227 | 9 | 9 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | | | | | | | 10 | 5 | 8 | 23 |
| 25 | 8911A0228 | 7 | 7 | 8 | ę | 7 | 7 | 8 | 8 | 8 | 8 | | | | | | | 8 | 5 | 9 | 22 |

| | 1 | 2 | 2 | ч | 5 | 6 | 7 | 8 | 9 | 10 | | | | DAI | REC | EXAM | TOTAL |
|--------------------------------|-----|------|----|----|------|----|-----|----|----|----|------|------|---|-----|-----|------|-------|
| [| , | | 3 | 8 | | 9 | 9 | 9 | 9 | 9 | | | | 9 | 5 | 7 | 21 |
| 26 18911A0230 | 8 | 8 | X | 3 | 1.02 | 10 | 10 | 10 | 10 | 10 | | | | 10 | 5 | 8 | 23 |
| 27 18911A0231 | 9 | 9 | 9 | | 9 | 9 | 9 | 9 | 9 | 9 | | | | 9 | 5 | 8 | 22 |
| 28 18911A0232 | 8 | 8 | 9 | 9 | | | | 9 | 9 | q | | | | 9 | 5 | 10 | 24 |
| 29 18911A0234 | 8 | 8 | 9 | 9 | q | 9 | 9 | q | 9 | 9 | | | | 9 | 5 | 7 | 21 |
| 30 18911A0237 | 8 | 9 | 9 | 9 | 9 | | 9 | 9 | 9 | 9 | | | | 9 | 5 | 7 | 21 |
| 31 18911A0238 | 8 | 8 | 9 | 9 | q | 9 | 9 | 9 | 9 | 9 | | | | 9 | 5 | 7 | 21 |
| 32 18911A0240 | 8 | 8 | 9 | 9 | | 9 | 9 | 9 | g | G | | | | 9 | 5 | 0 | 24 |
| 33 18911A0241 | 8 | 8 | 9 | 9 | 8 | | - 1 | | 10 | 10 | | | | 10 | 5 | 8 | 23 |
| 34 18911A0242 | ٩ | 9 | 10 | 10 | 10 | 10 | 10 | 10 | 8 | 8 | | | | 8 | 5 | 8 | 21 |
| 35 18911A0243 | 7 | 7 | 8 | 8 | 8 | 8 | | | | 10 | | | | 10 | 5 | 8 | 23 |
| 36 18911A0245 | 9 | 9 | 0 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | | | | 10 | 5 | 8 | 23 |
| 37 18911A0246 | 9 | 9 | 10 | 10 | 10 | 10 | 10 | 10 | | 10 | | | | 10 | 5 | 8 | 23 |
| 38 18911A0247 | 9 | 9 | 9 | 10 | 10 | 10 | 10 | 9 | 10 | 9 | | | | 9 | 5 | 7 | 21 |
| 39 18911A0248 | 8 | 8 | 8 | | | 10 | 1 | 10 | 10 | 10 | | | | 10 | 5 | 8 | 23 |
| 40 18911A0249 | 9 | 9 | 10 | 10 | 10 | 9 | 10 | 9 | 9 | 9 | | | | 9 | 5 | 8 | 22 |
| 41 18911A0250 42 18911A0252 | 8 | 89 | 9 | 9 | 9 | 10 | 9 | 10 | 10 | | | | | 10 | 5 | 8 | 23 |
| 42 18911A0232 43 18915A0216 | 9 | | 10 | 10 | 6 | 7 | 7 | 10 | 7 | 7 | | | | 7 | 5 | 8 | 20 |
| 44 19915A0201 | 9 | 1 g | 10 | 10 | 10 | | 10 | 10 | 10 | 10 | | | | 10 | 5 | 9 | 24 |
| 45 119915A0202 | a | 1 | 10 | 10 | 10 | 10 | 10 | 10 | | 10 | | | Ì | 10 | 5 | 8 | 23 |
| 10 19915A0203 | 8 | 8 | 9 | q | 3 | 9 | 9 | 9 | 9 | 9 | | | | 9 | 5 | 10 | 24 |
| 27 19915A0204 | 9 | - | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | | | | 10 | 5 | 8 | 23 |
| LN 119915A0205 | - | - | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | | | | 8 | 5 | 8 | 21 |
| 19 19915A0206 | 1 7 | - | 8 | 7 | 8 | 8 | 8 | 8 | 8 | 8 | | | | 8 | 5 | 8 | 21 |
| 50 119915A0207 | 1 1 | | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | | | | 10 | 5 | 8 | 23 |
| E. 10915A0268 | 11 | 9 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 18 | | | | 10 | 5 | 8 | 27 |
| 52 19915A0209 | | | 8 | 8 | 8 | 8 | S | ç | 8 | 8 | | | | 8 | 5 | 7 | 2.0 |
| 53 19915.00210 | | 9 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | | | | 0 | 5 | 8 | 23 |
| 54 10015A0211 | 9 | 9 | 10 | g | 10 | 10 | 10 | 10 | 10 | 10 | | | | 10 | 5 | 8 | 23 |
| 55 19915A0212 | 10 | > 10 | 10 | 10 | 9 | 10 | 10 | 10 | 10 | 10 | | | | 0 | 5 | 9 | 24 |
| 56 19915A0213 | 7 | 7 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | | | | 8 | 5 | | 23 |
| 57 19915A0214 | 9 | 8 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | | | | 9 | 95 | 7 | 24 |
| 58 19915A0215 | 7 | 7 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | | | | 8 | 5 | 9 | 22 |
| 59 19915A0216 | 10 | 9 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | | | | 10 | 15 | | 23 |

Name & Signature of the Faculty







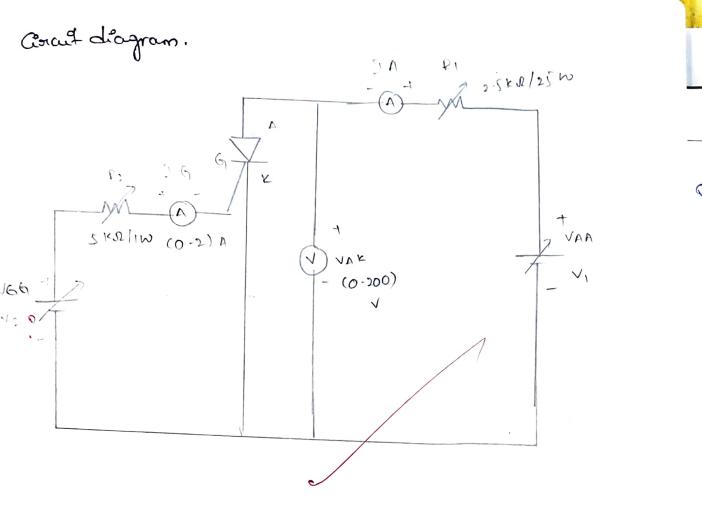
INDEX

| | Date | Name of the Experiment | Page No. | Remarks |
|--------|-----------|--|---------------|----------------------|
| S. No. | 26/2/21 | study of characturistics of SCR, MOSFET & IGBT | 1-4 | BRojel A. 8 [7/2] |
| સં | 26[7]21 | Gate firing circuite for scR's [R- Tougguing , RC - Tougguing & UJT | 8-13 | BRyil 26/7/21 |
| 3, | 26(7 [27 | Jouigquing] Single phase ac voltage correcolles with R&RL | <u>ા</u> બ-16 | BRyel APT21 |
| 4. | 2817121 | loads single phase fully contralled buidge consists with R & RI loads | (7-19 | BRjilsoldy AD |
| 5 | . 28[-1]2 | De Jones ichoppie with R & RL bads | | BRight 20 Folor |
| 6 | 28/7/21 | single phase parallel invisiter with R & RL loads | 23-24 | BR J 30/F/21 |
| | | | | |

INDEX

| S. No. | Date | Name of the Experiment | Page No. | Remarks |
|------------|---------|--|----------|----------------------|
| н . | | single phase cyclo-connectee with R&RL bads | 52-53 | BR jerl At 2/8/21 |
| S. | 3017121 | single phase Services inverter with R&RI loads | 28-30 | 8 hjl 18/21 |
| 9. | 3017(21 | Simulation of 1-0 full consulty using RLE loads & 1-0 AC voltage controlles using RLE loads | 31-36 | BRije At |
| 10 . | 3017[2] | simulation of 1-d vinverter with pion control | 37-39 | BRill At 18/21 |
| | | | | ~ |
| | | | | |
| | | | | |





J

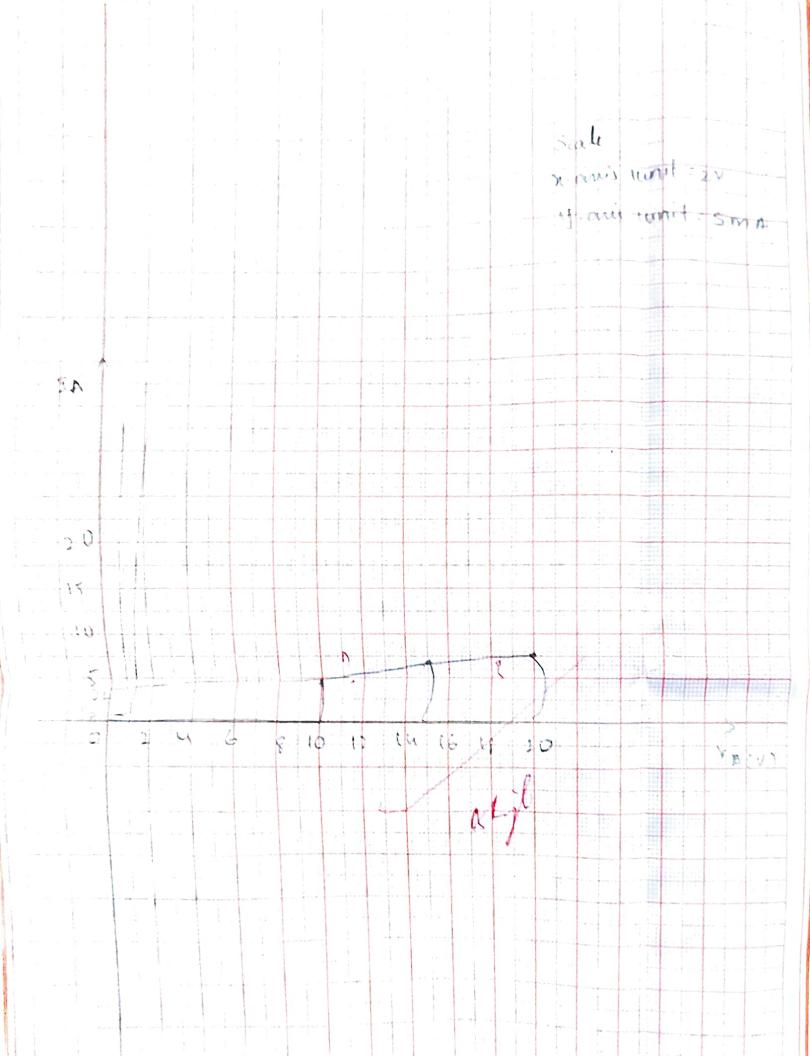
Title: 1. static charactuistice of SCR. Date: 26/7/21 Page No.: 1 dim: 20 plot the charactuistics of SCR and its find the tatching & holding currents. Apparatus: 1. SCR charactuistics study unit. 2. Meter unit - Voltmeter CO-20)~ - INO Ammeter CO-20)~ - INO Ammeter CO-200 mA - INO

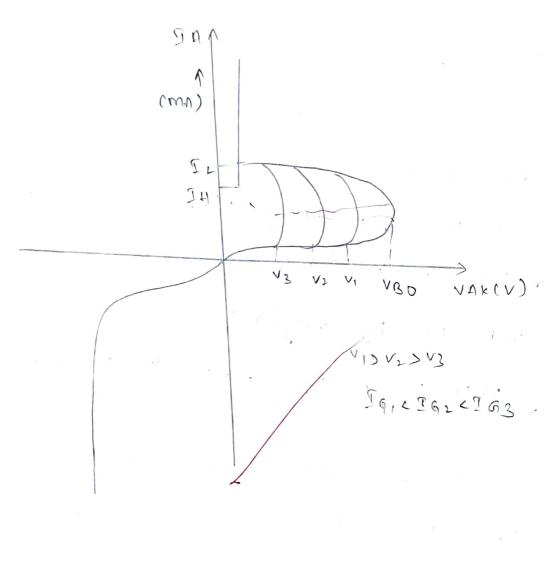
Jhuby: SCR is a seri conductor device which raits cars an electueonic switch. It controls the comount of poince fed to load. SCR is most populas member of thyuitor family. It ris a four days there justion pNPN device having there terminals & und as a Switch. SCR hou woo statu i e it dou not Conduct & conducts heavily.

Obsenvations.

| VAK (V) | IG (ma) | (mn) | (v) | (ma) | In (ma) | (VAIK) | | IA (mA) |
|------------|------------|-------|------|---------|------------|--------|----------|------------|
| (0) | 0.001 | Ö | 15 | 0 = 002 | O | 20 | 0.002 | 0 |
| 10 | 0-004 | 0 | 15 | 0 .003 | 0 | 20 | 0.003 | 0 |
| 10 | 0.005 | 0 | 14.9 | 0.004 | 0 | 20 | . 0 0004 | D . |
| 10 | 0.006 | 0 | 14.9 | 0005 | 0 | 20 | 0.002 | 0 |
| 9.3 | 0007 | 0 • 1 | 14-9 | 0.006 | 0 | 20 | 0-006 | 6 |
| 6.) | 0.008 | 3.9 | 057 | 6000) | 6.3 | 19.9 | 6-00-2 | 0 |
| 0-7 | 0-009 | 3.6 | 6.7 | 0=008 | 6.4 | 0) | 00008 | 8.6 |
| | 0-0 1 | 3.9 | 0.7 | 0.009 | 6.4 | 0) | 0.001 | 8.6 |
| | | | | N N | | | | |

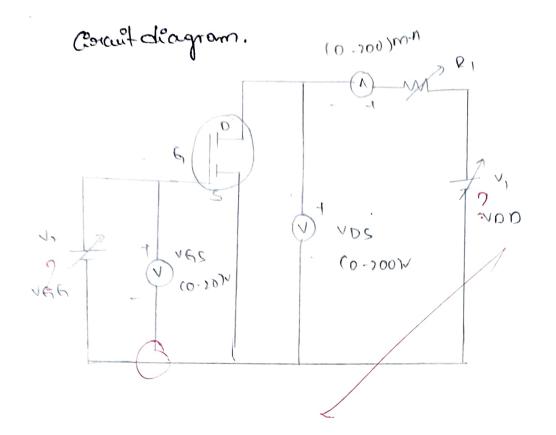
l



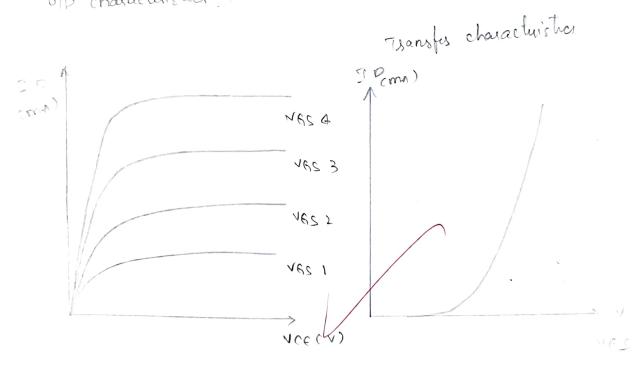


ł

Date : Page No. : 3 Result: us have done the characteristic of SCR and deturnined the latching & holding current. Bry 28 8/21



olp characteristici :



Date : 26-7-21 Title: characturistice of MOSFET Page No.: Y dim: 10 plot the duain and duanconductance characteristic of MOSFET Apparatus :-1. MOSFET characturistice study unit. Voltmetu CO-20)V - INO 2. Meter unit voltmetu co-200)v - 1NO Ammetu CO-2007MA - INO 3. patch caseds . A ponces MOSFET that there ileminate called Theory ? . duain, source and Gate. MOSFET is a voltage controlled device & ite opuration depends on flow of majority carries only. MOSFET is unipolar denice. The control signal & base cursent recognized in MOSFET This is because the gate circuit is less. umpedance in MOSFET enteurnely high.

ole characteristice

| VGS | - 2 V | VGG | 22-3V | Ves | 3.11 | - |
|-----------|--------|---------|---------|--------|--------|----|
| NOS (N) | JO(MA) | VOS(V) | ID (ma) | NDS(V) | Jo(mA) | |
| 0.01 | 0.0 | 2.1 | O | 2.75 | ١٠٥ | |
| 2 . 7 | 0.1 | 2-8 | 0.1 | 2-29 | 0.1 | ¢. |
| 3-85 | 0.2 | 2.9 | 0.3 | 2-13 | 0 2 | |
| 3.08 | 0.5 | 3.0 | 0.6 | 2.94 | 0.5 | |
| | 0.6 | 3.2 | 0.7 | 3.0. | 0.8 | • |
| 3.2 | | 3.4 | 0.7 | 2.1 | 0.9 | |
| 4.0 | 0.6 | | 0.3 | 4 | 0 · 9 | |
| 5.0 | 0.6 | 5 | | | | |
| TISanster | chasac | luitics | | | | с |

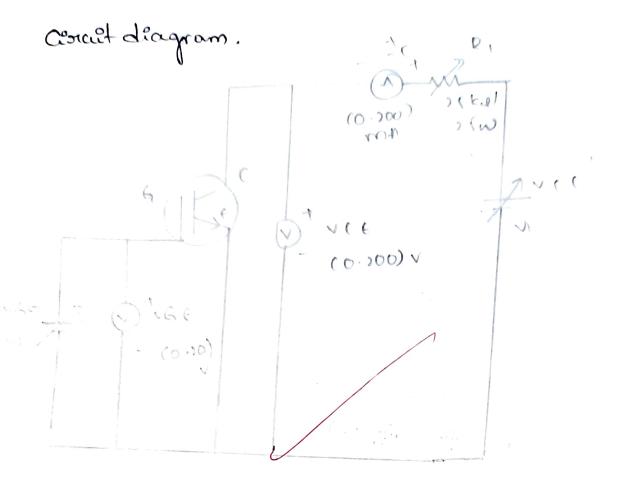
•

risansfu chasactuities

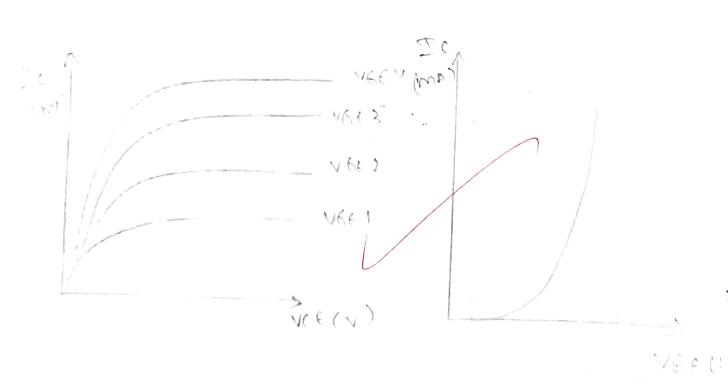
| 2 D V | = 2·5 V | | |
|-------------|---------|--|----|
| VGC (V) | Jo(mA) | | |
| 1-23 2-7 | 0 | | |
| 2.9 | 0.4 | | |
| 3-0 | 0.4 | | |
| 3.12 | 0.9 | | L. |

| | | - | | the second strangenetics. | | | | | | | | | | | | | | | |
|------|----|---|-----|---------------------------|----|---|-----|-----|----------------|----|---|----------------------|---|---------------------------------|---|-----|-------|------|-----|
| | 7 | | t. | 0 | Ĝ | | | 0 | | | | | | | | | | | |
| | 1 | 2 | | - | 1 | | 1 | | | 3 | 0 | 0 | C | - | | -1 | - | - | |
| | | | | | 6 | | 2 | - | | Ŧ | | 3 | | 5 | • 6 | -8 | -5 | | 10 |
| | - | | | | | | | - | | | 1 | | | | | 1 | - | 0.00 | |
| 0 | | | | | | | | | | | | 2 | | | | | | | |
| ~ | | | | | 1 | | | 1 | 0 | | | 2 | | | | | | | |
| 4 | | | | 1 - | | | : | | 5 | | | 2 | - | | | 1 | - | | |
| + | | | | | | | 1-1 | | | 1 | | | | | | 2 | - | | |
| | | | | | | | | | | 1 | | | | | | | 1 | | |
| | | | | | | | | | ъC | | | | - | - | | | - | | |
| 1 | | 1 | | | | | | | | | | | ~ | | | | - | | |
| | | | | _ | | | | | . 1 | | | | | | | | | | 1 |
| 7 | | | | | | | | | 1 | | | | | | | | -10 | | |
| | - | | | | | - | : E | | | | | | | | + | 1 : | | | - |
| 1 | | | 1 | 1 | 17 | | | | | | | | | | | | | | |
| | / | | | | | | | | • | | | | | | | | - | | n |
| | 1 | | | - | | | | | 0 | | | | | | | | | | |
| 2 | | / | | | | | | | | | | | | | | | | | C |
| | | 5 | | | | | 11. | | 2 | P | | ++ ++ ++ ++ | | | | -7 | | | h |
| 5 | | | | | 1 | | | | - < | | | | | | | 1 | | | |
| | | | | | | | | | | | | | | | | | | | 10 |
| cn . | | | | | 1 | Y | | | VJ- | | | | | | | | | | - |
| | | | | | | D | | | | | | | | | | | | 4 | |
| | 1. | | | 11 | | | | | 0 | | | | | | | | | | |
| -0- | 3 | | | | | > | | | 3 | | | | | | | | | | t |
| | A | | / | | | | | | , | | | | | | | | | | |
| 5 | 1 | | | | | 2 | | | 5 | | | | | | | | | | |
| | A | | | | | 3 | | | | | | | | | | | | | |
| SC | | | | | | Ň | | | | 0 | | | | | | | | | |
| 1 | | | | | | | | | 0 | | | | | | | | | | |
| 4 | | | | | | | | | | | | | | | | | | | |
| 5 | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | Ę | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | • | | | | | | | | | | |
| | | | | | | | | | \overline{o} | | | | | | | | V | | |
| | | | | | | | | | | V | | | | | | | 6 | | |
| | | | | | 11 | | | | | 6 | | | | | | | | | |
| | | | | | | | | | | \$ | | | V | | | | | | |
| 6 | | | | | | | | | | | | | | | | | 2 | | |
| | | | | | | | | | | | | > | | | | | -2 | 1 | X |
| | | | | | | | | | | | | | | | | | ~ | 0 | |
| 6 | | | 111 | + | | | | | | | | | | | | | | V | a |
| 5 | | | | | | | | | | | | | | | | | | n | M |
| | | | | | | | | | | | | | | | | | | | A |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | " | |
| | | | | | | | | | | | | | | | | | | .r | in |
| | | | | | | | | | | | | | | | | | | | ,1 |
| | | | | | | | | | | | | | | | | | • • • | | |
| | | | | | | | | / 1 | | | | | | | | | | 0 | Ō. |
| / (| | | | | | - | | | 2 | | | | | | | | | | |
| 2 | | | | | | | | | | | | | | | | | | ſ | 5.5 |
| 7 | | | | | | | | | | | | | - | + + + - + + + + + + + + + + + + | | | | t | 1 |

Date : Page No. : 5 Title : Peroceoluse !a) Duain l'output characteristice :-1. Give the connections as shown in cucuit drag. with melus. 2. stonely vary v2 & adjust VGS=2V. 3. Vary V, in stips & note VOS & ID. 4. Repeal peroadure VGS = 2-7V & 2.9V 5. plot VDS VSID 18 diffuent VGS values. 6) Teransfie chasachristice :). Set VDS = 2.5V ley varying V, 2) By varying ve in steps, note vas & ID the each step, adjust VOS = 2.5V & role VGS VS JD values. 3) plot VGS VS JD to VDS. Perult: we have studied duain & duanconductana characteristic of taosFET. Bhogil 28/7/21 (A



woodd work



Date : 26-7-21 Title: charactuistice of IGBT. Page No.: 6 Aim: 10 plot the collecter & twantfer charactuistics of IGBT Apparatur :-1. IGBT characteristics study unit. - 1NO voltmeter CO-20) V 2. Meter unit -- INO vollimetre (0-200) Ammiles (0-200)MA - INO. 3. patch cosds. procedure !a) collectés characteristics :-) give connections as showen in ciscuit diaguam. 2) slowly vary v2 & adjust VGE = 4V. 3) NOW Vary V, in steps & note down vice & Ic for each step. 4) plot vce & Ic for different values of vee.

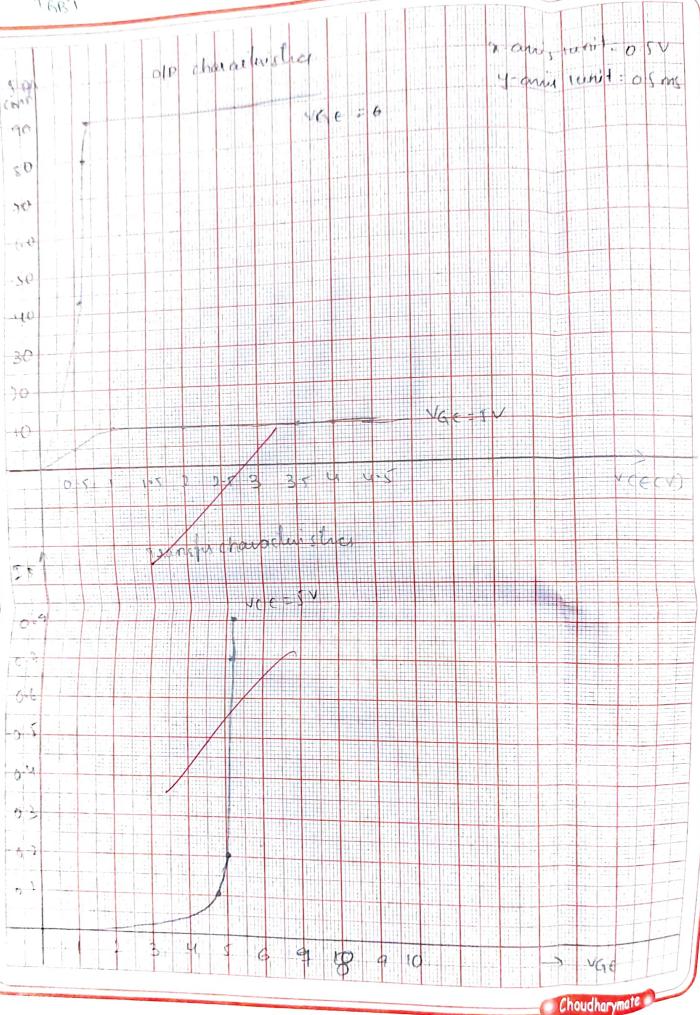
JP charactuistion

| VG | E : 2 V | ×6e = | 3. V | vse : | 4 V |
|------|--|---------------------------------------|--------|--------|--------|
| VECO | Je (ma) | vce (v) | Icoma) | VCECK) | Icema) |
| 1.5 | 0 | 0.5 | 03 | 0.4 | 0.3 |
| 2-1 | 0 | 1.0 | 0.5 | 0.5 | 0.5 |
| 39 | 0 | 0.0 | 0.5 | 0.6 | 01.3 |
| 40 | 0 | 1.5 | 0.5 | 6.2 | 6.3 |
| 5-9 | 0 | Ч | 0.5 | 0.8 | 9.7 |
| • | 0 | 4.5 | 0.5 | , | 7 |
| | an shi sheka kata ta ta ta ta ta ta ta | percyana, styliggymetrika, throne and | 2 | | |

bonsta charactuities

| NCE > | 2 V |
|-------------------|--------|
| ∼ ∈ € | tecmai |
| 1-21 2-03 3 | |
| 4.2 | 0.3 |
| 5-1 6-02 7 | 0-9 |



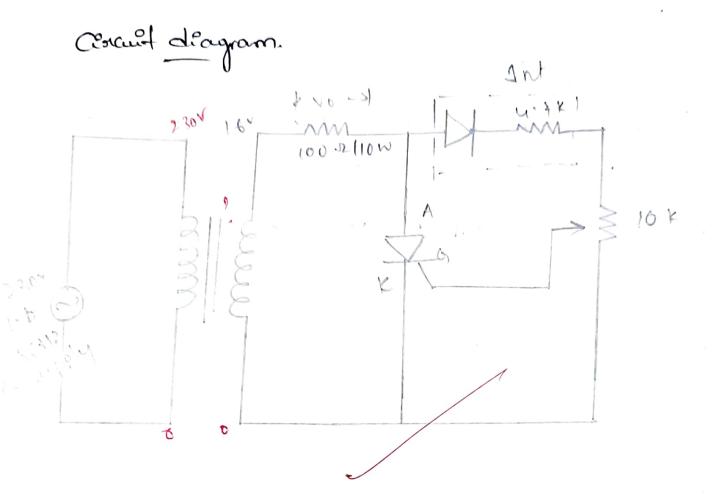


Title :

7

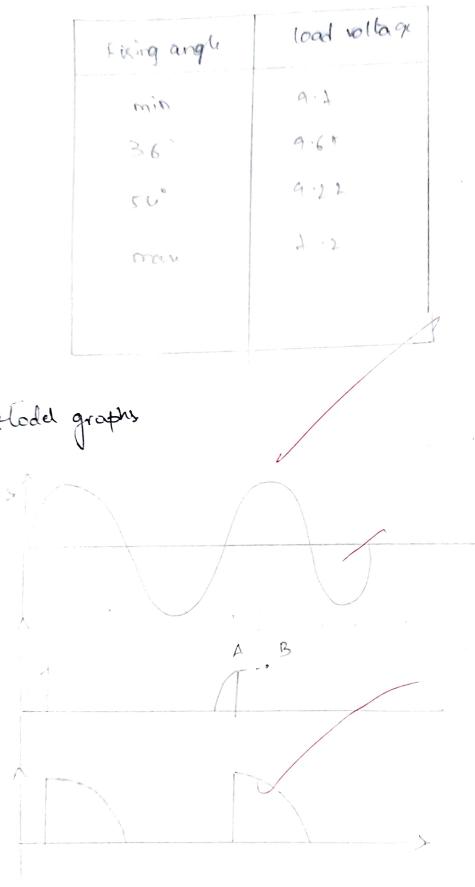
b) Tuansfu charactuistice:) set vce = 5 ley vasying v, 2) By varying v2 in steps, note vare & Ic for each step, adjust vec = 5v & note vee & ID. 3) plot voe vs Ic to different values of vce.

Result: no have studied the characteristice of collector & Juanifie of JGBT BR 1 28 7/29

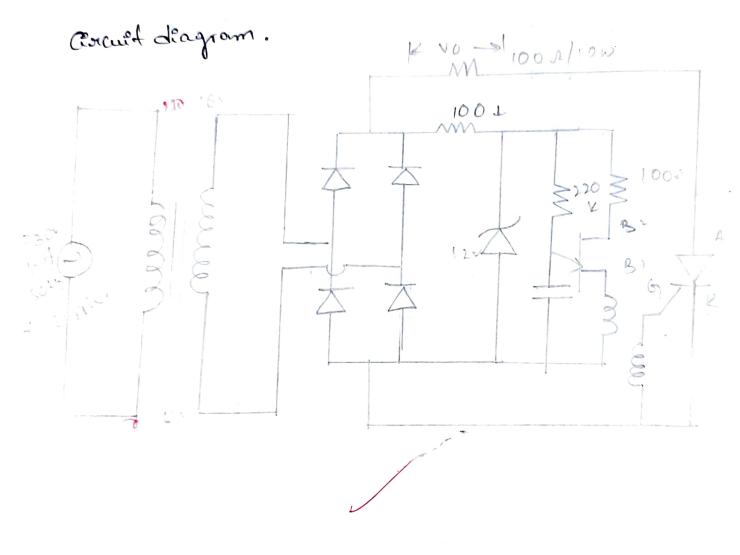


Date : 26-7-2(Title: 2. Gate fixing circuite for scrs Page No. : 8 [R. Tougquing, Re thigging & UIT touggaing] dim: 10 study the amplitude control of scr with R duigquing. Apparatus !-1. SCR duigquing module. CRO 2. patch cards 3. 4. Multimeter. SCRS an neidely und as controlled recipiers Theory ! to obtain variable De voltage from find Ac source. SCP conducts like a diode only when ile ranode is positive wirto cathode and on application of sufficient gale current at specified gale to cathode voltage.

Observations.



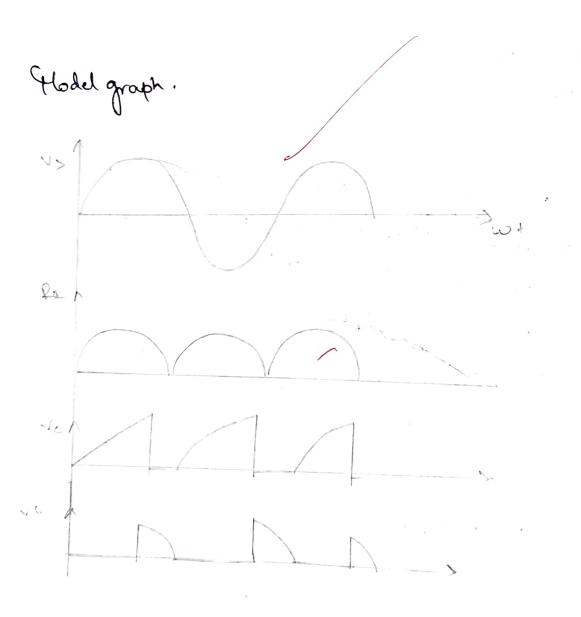
Date : Page No. : 9 Title : perocidure !.) give the connections as per the circuit diaguam. 2) switch on module. 3) set the potentiometer to any pasticular position & obscure the vicineforme of VIN, VO, VT, VP on CRO s note waveforme 4) vasy potentiometer & note fixing angle & cossesponding load-voltage using multimete. Results: Amplitude control of SCR with R. tingging was studied BRy 28 7/21

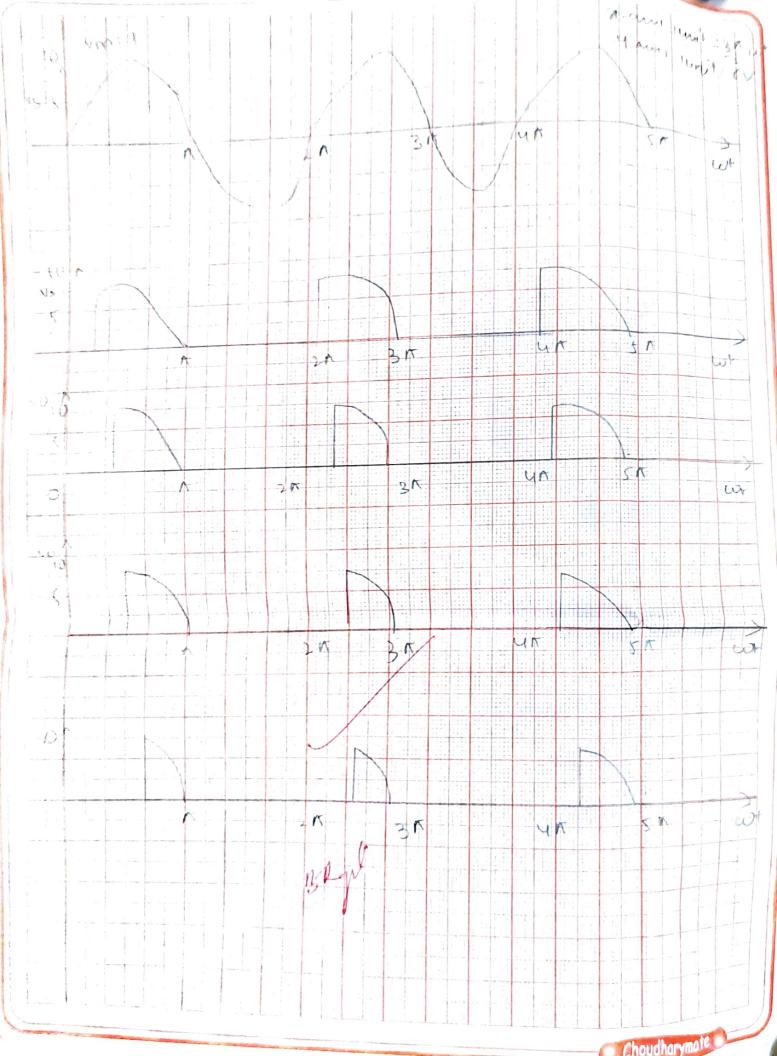


and the second s

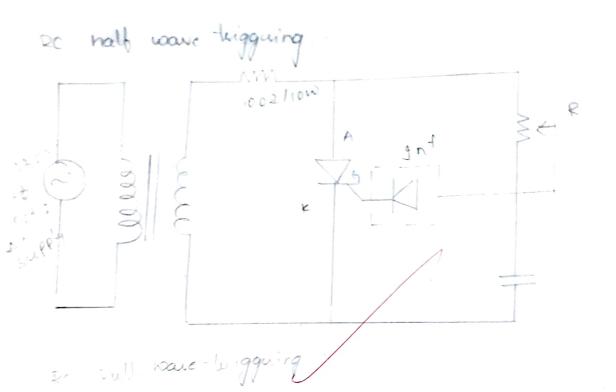
| E. |
|--|
| Title: UT desigguing cucuit Date : 26-7-21 Page No.: (0 |
| Aim: Jo construct & study UST tuggering circuit to |
| tuiggue an SCR. |
| Apparatus: 1. SCR Tonigguing module: |
| 2. cRo 3. patch Cards |
| 4. multimeter. |
| Thedy: WIT worke as relavation ascillator output |
| pulses of variable time period an possible by |
| have all worthat the work of the |
| ily amploying a consult of |
| charging a capacitor by a overistor. The Re network can be easily employed to |
| abtain alp pulses. |

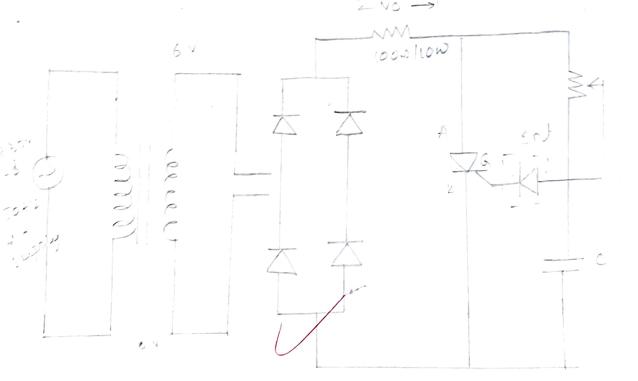
| Obsesivation | 18 |
|---------------------|--------------|
| Fising angle (x) | Load voltage |
| 19 | A · 4 |
| 36 | 7 |
| 90 | 4.1 |
| 16) | 0 - 1 |



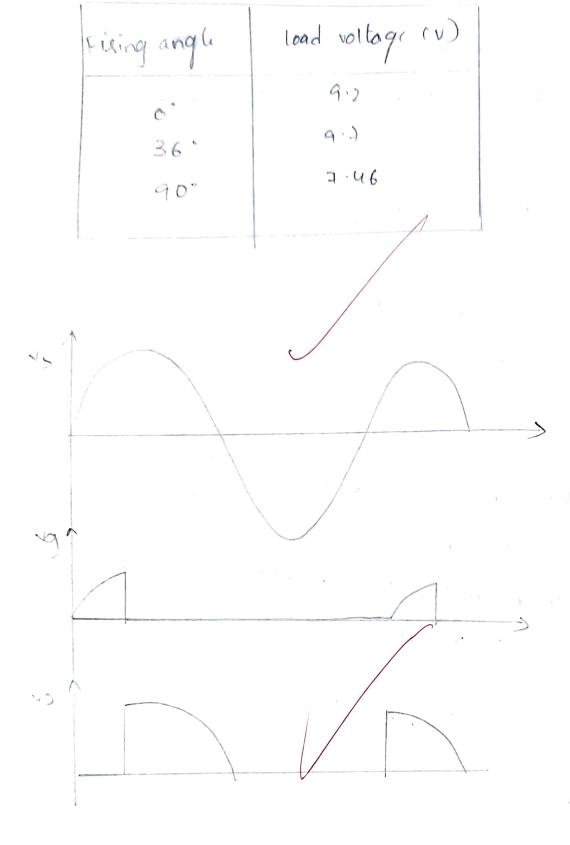


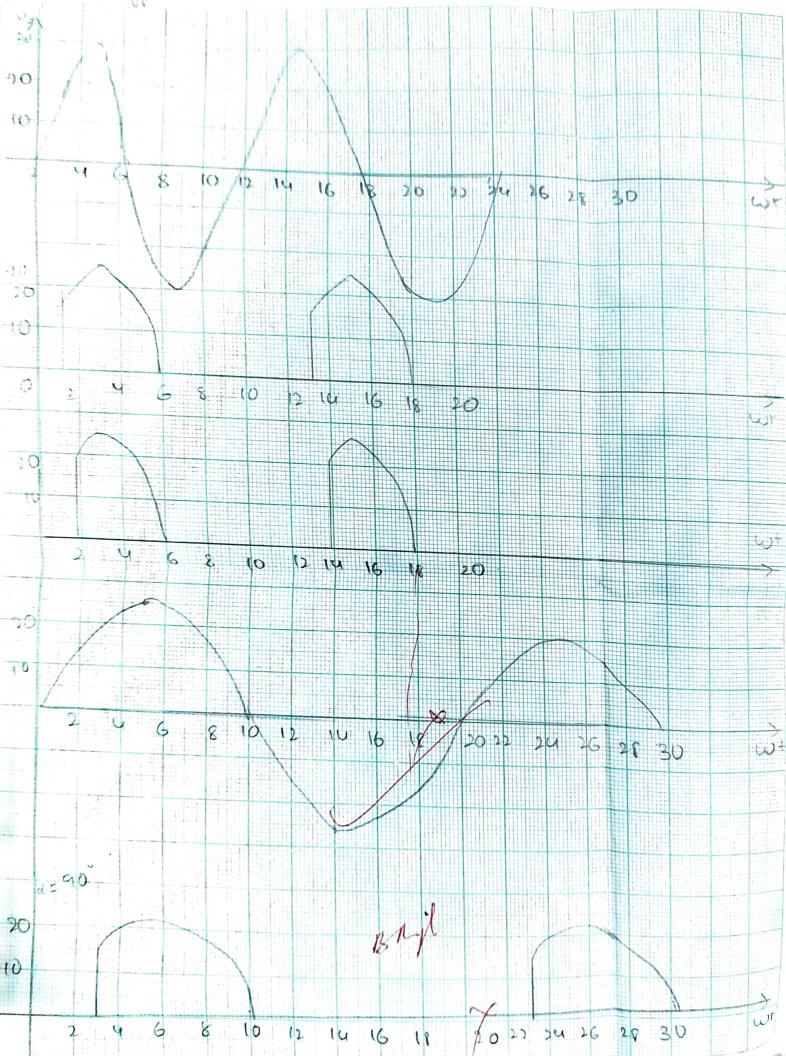
Date : Page No. : 1) Title : parocedure !.) fine the connectione as per circuit diaguam. 2) switch on the module 3) set potentionnelle & abscurre the warreforme VIN, NO, NT, NP, ND, NZ, NC ON CRO 3 note Wareforme. 4) By varying R, note down the firing angle & load voltage The UIT Luiggering circuit de Luigger an Result ? SCR was studied. BR/ 28/7/21





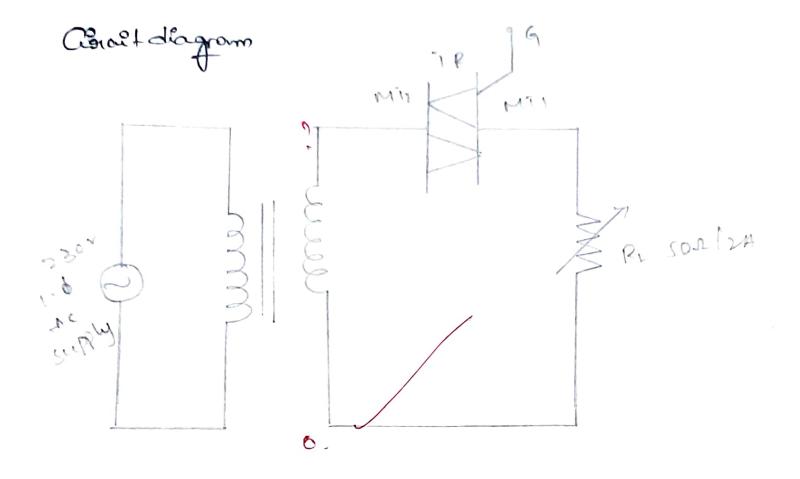
| Title: Rc Jeuggueing | Date : 26/ナ/虹1 Page No.: 1ン |
|--|--------------------------------|
| Aim: 30 study the phase contuol of | SCR ley RC |
| twiggesing . | |
| Apparatur: 1. SER derigguing module | , |
| d' CKU | |
| 3. patch casds | |
| A. Multimeter | |
|) Give the connections as per ci | icuit diaguam. |
| 2) switch ON the module. | waveform of |
| 3) set potentiometer to our of a vino, vo, vi, vp, vc on cro & | role varefams. |
| 4) vary the potentiometer & note a cossesponding load voltage using | loven the |





Date : Result: phan contuol of SCR with RC Jugging Was studied. Page No.: 3 Title : A BRgidstala





Date : 26-7-21 Title: 3- single phase Ac vollage contuolly Page No.: 14 Aim: 30 constand single phase AC voltage contradher reincuit & to study ite operation with R & RL loads. Apparatus :-1. Single phase ac voltage contuelles unit. 2. Loading Rheostat (50 2/ JA) 3° boading Anducto (0-150mill 2A) 4. Digital meettimeter 5. CRO 6 · patch casds . Jhusy: A voltage controthe connext fixed alturating voltoge directly to variable alturnating voltage without charge in furquency. some of main application of Ac voltage controller are donestic and industrial heating.

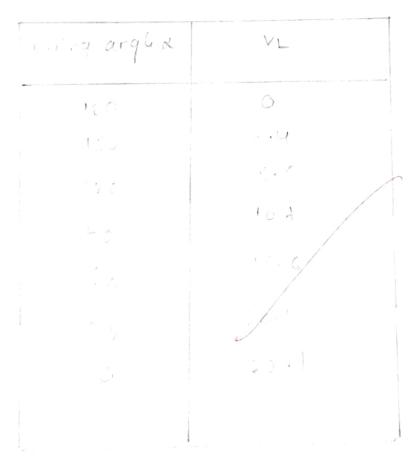
observations

Ŕ

×10 - 22 3×

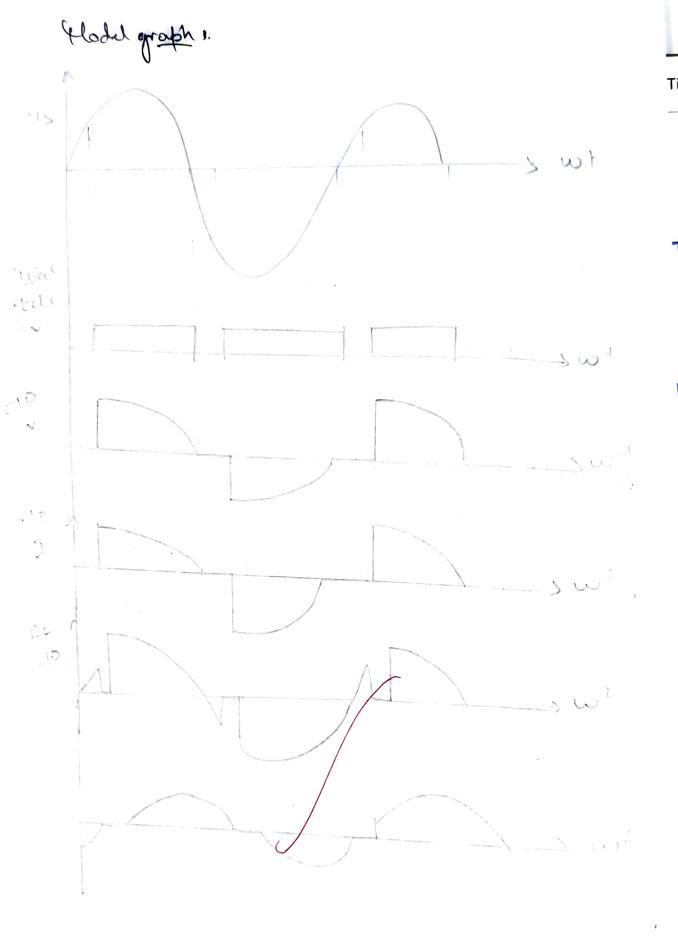
| a iting angle a | 4 |
|-----------------|------|
| 110 | Ô. |
| 150 | Ô S |
| 120 | 6 6 |
| 90 | 9.9 |
| 60 | 149 |
| 30 | 6 |
| 0 | 52-3 |

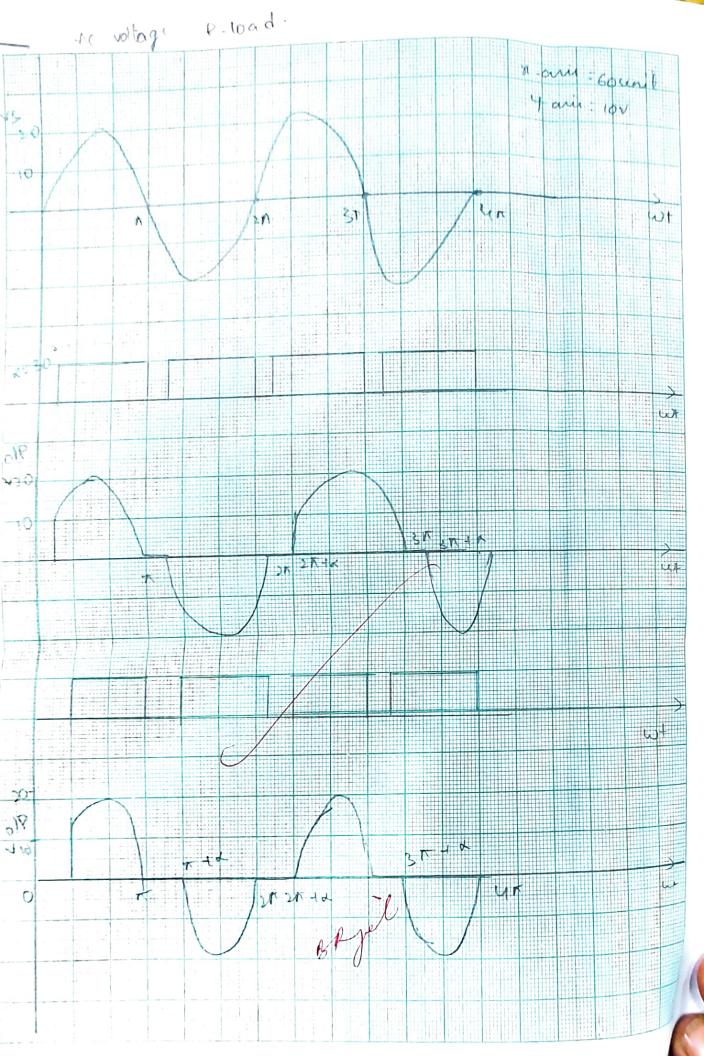
FL Spridely



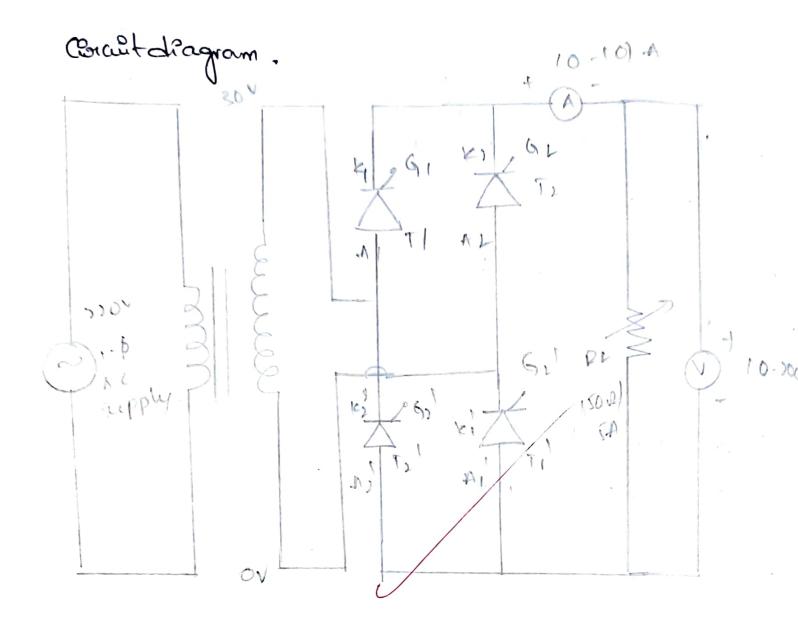
Perocedure :-1) switch on the main supply to unit. a) give the connections as shown in ciscuit diaguam for single phase Ac voltage controller resing ser 1 TRIAC connect the Ac supply to circuit through stup down TIF. 3) connect the dwiggers ofp's 7, \$72 fears firing circuit to SER [TRIAC. Selic Scr] TRIAC Switch to SCR for Ac voltage 4) keeping firing angle knob at some intermediate position, sweitch ON the slip down TIF supply & tuiggre Olp's & observe the olp voltage wareform 5) vary the firingle angle & measure the load voltage using meltimete. c) Fôs the single phane -ne voltage controlles.

Title :





Date : Title : Page No. : 16 for RI load, connect the inductor in series with load f. 7) Repeat above steps to ac voltage controlles with RI load. Result: A single phase ac voltage contecolles was constructed & its operation with R& PL load is observed BH 28 8/2121



| Title: 4. Single phase fully controlled Date : 28-7-21 Page No.: 17 |
|--|
| Beudge consulter |
| |
| dim: 10 construct single phase fully contradud |
| devidge connectu circuit & do study its operation with |
| levolge |
| R S. RI Load. |
| |
| Appairates :- |
|) single phase fully controlled buidge convertes |
| pouce unit |
| pour converte fing unit |
| J) single phase feeling contractions with - appings. |
| pour unit: single phase fully controlled beidge converter fingunit single phase fully control beidge converter fully con |
| 4) wading Rhuostal - 150 215n. |
| |
| 5) Inductor - 150 mtil 5 million |
| E) CRO |
| 7) patch caude |
| the fous aums of |
| Theory: In beidge contretter, un quoitche. This |
| Scription connected as control switche. This |
| Schis were conhected in beidge as all the is called Fully controlled beidge as all the |
| us called rung - heider from. |
| SERS vous connected in bridge form. |
| |

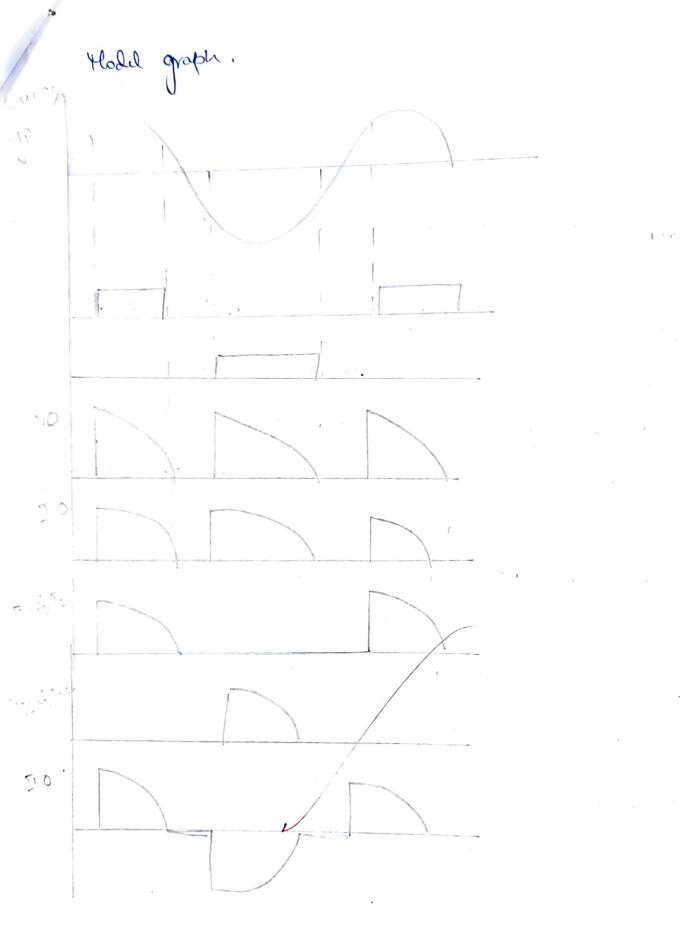
Observation. R. load

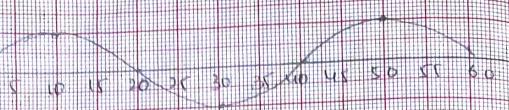
Vi: Vm (1+ cora) Fining angle JK ∇_1 K Ô 186 0 0 0.05 1.2 150 2 6.4 190 0 22 10 12-9 (\rightarrow) 90 0.35 19/3 60 6.50 22 24.05 24 0.16 30 : Mª 13 2517 0.56 \bigcirc

CL

VL= Vm(1-1 cord) Lung angle VL T.L. èd; λ 180 \bigcirc 0 0 1 150 105 0.01 6 120 5-6 0-12 11 90 11.6 0.14 21 60 1.1.5 0.43 24 2:0 6.5 21.2 25 ()02.3

| using firing culture (1, 1 - 1, 1) in pour circuit. 6) switch on main supply to firing circuit. 6) switch on MCB in pour circuit & switch on trigger olp's in firing unit. 7) keep the firing angle of some position & decow waveforms in Vin & Vo. 8) duare the waveforms across the load for | |
|---|--|
| eine the connections as stated in the tate of connect sov itapping of wolation TIF secondary do pound circuit. connect R-L load (150 21 5A) between the olp points. connect the duigger pulses from connectur using fixing circuit TI, Ti' & Ti, Ti' to cossuponding SCR'S (Ti' T, '& Ti, Ti') in pound cacuit. switch on main supply to fixing circuit. switch on main supply to fixing circuit. switch on MCB in pound circuit & switch on utigger olp's win fixing unit. keep the fixing angle ad some position & decaw waveforms in Vin & vo. duare the waveforms across the load fet | |
| 6) switch ON MICE un pours and strigger olp's in firing unit. 7) keep the firing angle ad some position S decour wavefams in Vin S vo. 8) duare the wavefams across the load for | puocedun: Aim the connections as shown in circuit diagram Aim the connections as shown in circuit diagram connect 800 dapping of wolation TIF secondary do pours circuit. connect R-L load (150 21 5 A) between the olp points. connect the desigger pulses from connects connect the desigger pulses from connects and fixing circuit Ti, Ti & Ti, Ti' to connect servers (Ti', Ti' & Ti, Ti') in pours circuit. |
| a) keep the fining angle of some positions decoup waveforms in vin & vo. a) decoup the waveforms across the load for | 6) switch ON MICB un pours triggers ofp's un figing unit. |
| 8) duant the waveforms across the load ges | 7) keep the fining angle of some positions decous maneforms in Nin & VO. |
| | 8) duans the waveforms across the board for diffuent firing angle & note ofp voltage & Ofp current from voltmeter & ammity. |

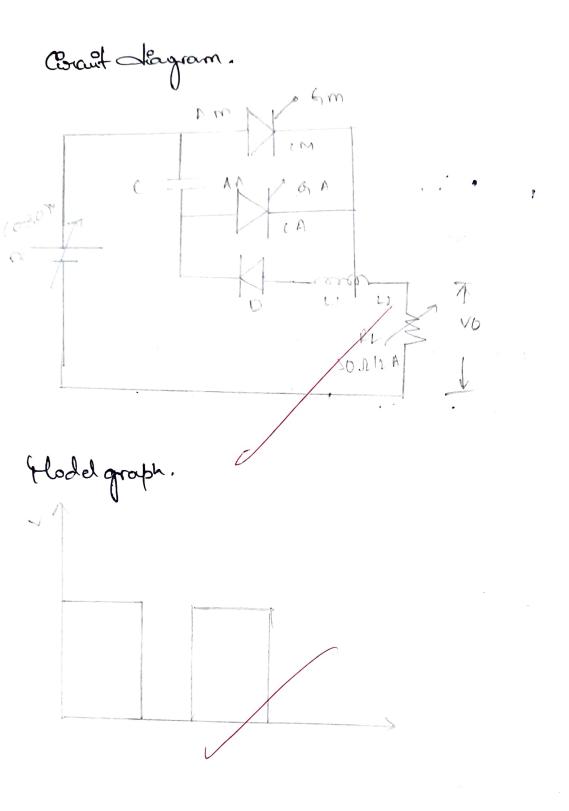




5n

1/1/

Date : Title : Page No. : 19 1) At vary filing angle, note the old waveform vo & to different firing angle note of p voltage & OP ausent from volbriche & ammélie. Result: A 1-0 fully controlled buidge constanted s its operation with R & RL hard observed. BKg 20/7/24



Date : 28/-1121 Title: 5. DC Jones choppes with R and Page No. : 20 RL loads dim: Jo construct Jone chopper circuit & to study ile operation with R & RI load. Apparatus :-1. choppes ponies module. 2. choppes firing unit. Regulated points supply (0-30)~ 3. A. loading pheostat (50,212A) Enducta - 50 mH/2A Ś. 6. Digital multimètre J. CRO 8 patch casds. shudy: choppes contacts fined De voltage to Variable De voltage. The De to De convertus have gained popularity in modun industry. some practical applications of De to De connentus include asmature voltage control of DC motors conneiling one De voltage level to another titlel.

Observations

| ON | TOFF | (\checkmark) | | 3 |
|----|------|----------------|------------|-----|
| | 6 | 9 | | |
| 1 | 3 | 9 | с. Р. С | · • |
| | e . | 9 | | |
| 2 | 9 | 9 | | |
| 4 | 18 | 1 | | |
| | | | | |

Observations.

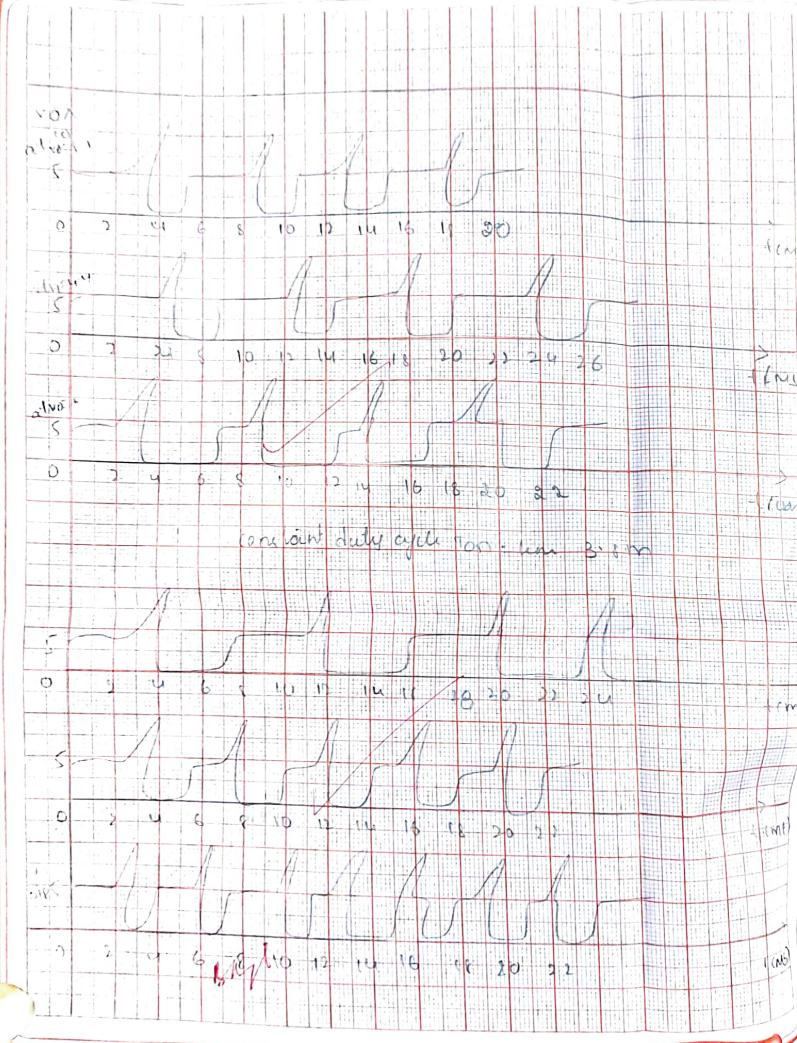
| Exiquency | 50 M | TOFF | \vee | |
|-----------------------------|------------------|------------------|-------------|--|
| 66 ez:6 111.1. 125 | 6 5 4 3 | 9 7 5 5 | 9 9 9 | |

.

10

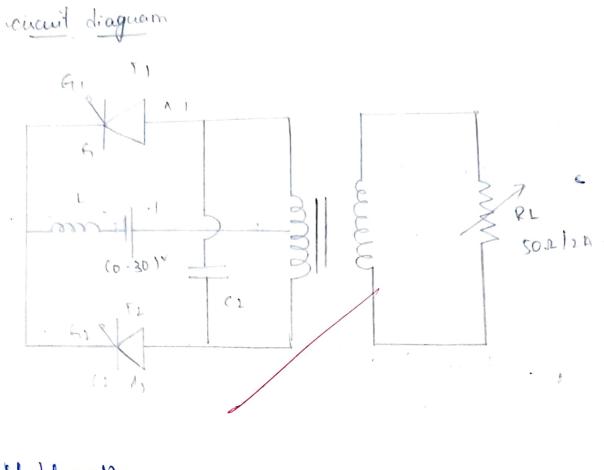
ł

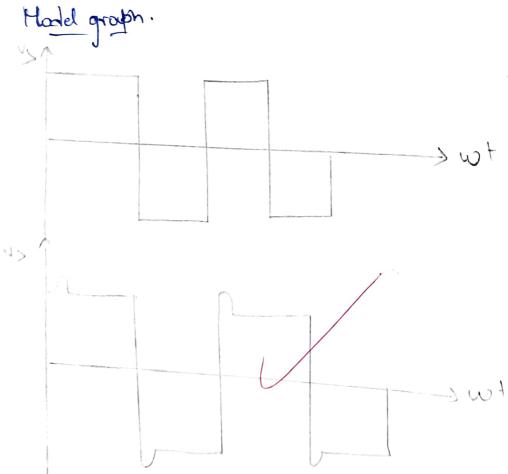
| Title : Date : Page No. : 21 |
|---|
| Perocrohure!) fime connections as per circuit diagram with R load. |
| 2) connect Gali certhode terminale of sep's to respective points on firing unit. |
| 3) keep the fuequency knob & duty ratio knob at some intermediate position. |
| 2) set DC pours supply to 30v & switch on the |
| Oc pours supply to chopper. |
| s) obsume vo, vr, .VTz, VPI, VPZ, VC waveforme on cRO & note down the cossuporating waveforme. |
| 6) keeping the funguarcy const vary duty taych |
| un slope & note Ton, TOFF & load voltage |
| fs cach step. |



Chaudhammate

Date : Title : Page No.:)) 3. Repeat step 6 day varying feliquency & keeping duty satio constant. 8 connect Re load & note old vo & supear steps Repult: we have studied the characteristic of D.c Jones chopper. BRay 20 7/21



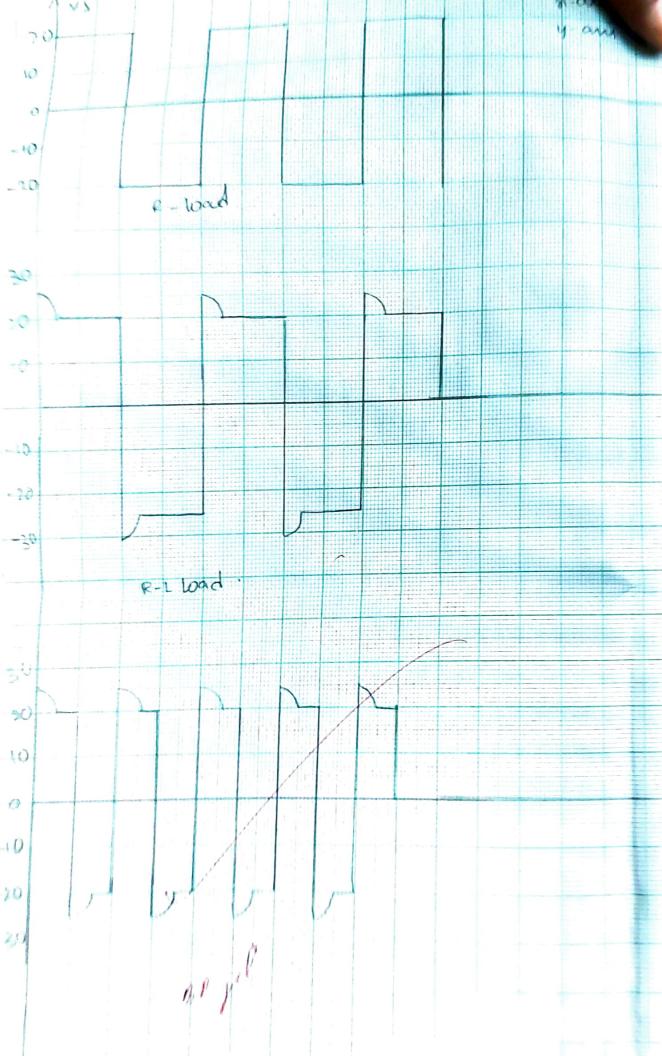




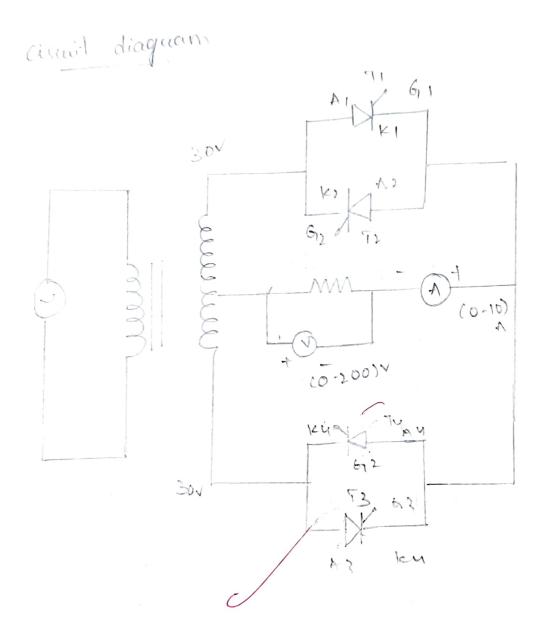
CIP (V) Luquinay 63-212 69.25 62-812 91 49 64.811 10 16

in load

| England | opvoltage | . VT | VC |
|-----------|-----------|-------|------|
| 109.14 | 38.12 | 53612 | 36.6 |
| E-) · · · | 3-1-81 | 29-1 | 36.6 |
| | | | |



Date : Title : Page No. : 24 p.excedure !.) give the connections as shown in circuit diagram. a) connect the firing unit ils main unit. 3) Adjust the DC supply to 13 v & switch on the main unit & firing unit. 4) set the funquency at a particular value & observe the load voltage variefame No. VT, NT2, VP1, VP2, VC on cro. 5 note waneforms. s) By varying the frequency, note OIP ac voltage using meltimetre 6) conned to load & note ofp vo-7) Repeat Stip 5 fr PL load. Result: Hence studied the 1-0 parallel vinnetter with R & RL Load. \$ 30 7 21



·

. . /

Date : 30-7-21 Title: 7. Single phase cyclo- connecter Page No.: 15 with R and RL loads Aim: 30 construct la single phase cyclo conviste aicuit & to study its operation with R & RL loads . Apparatus:) cycloconverter ponus unit. 2) cyclo connecte pising unit. 3) single phase isolation duansfame 4) hoading subcostat = 502121. (0- 150 m+1 15A) s) Inductor 6) Digital multimetu A) CRO 6) patch cards Jhudy? - A ciscuit which connuite unput pours af one quequency to output pomes at diffuent fuequency with on Stage conversion is called ca cycle conneitre cycle conneitre ase used in speed control of high pomes no drives, induction heating de

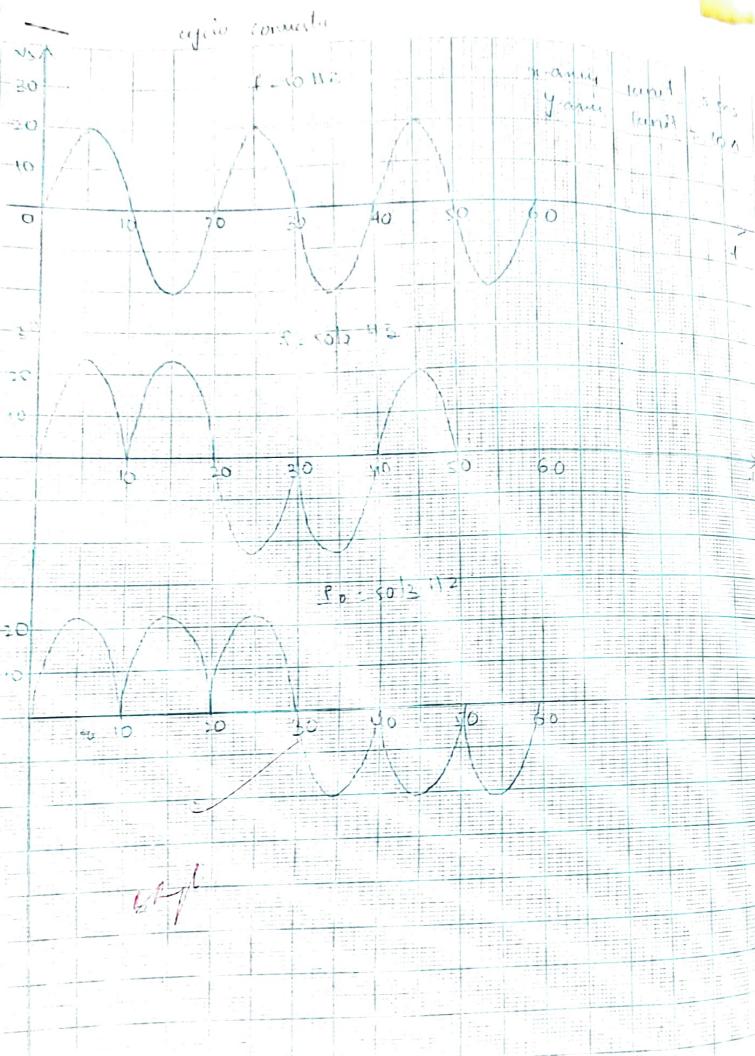
Observations

R

| | 6 | ve tlage | tursent | |
|---|--------------------|----------|---------|-------|
| | . ٩, | 27. 1 | 0.22 | |
| | £ 5 2 | 27 | 0,23 | |
| | 01.56 | 2 | 0.22 | , |
| | fs a | 27 | 0.2 | 2 |
| L | | | | |
| | freque | Ń | T | |
| | Î | 5.7.) | 0. | 22 |
| | ¢ 5. | 2.7 · 2 | 0 | . 2 2 |
| | GR | 2-9-2 | 0 | > 2.) |
| | P. Lin | 2 5 - 1 | 0. | 2.2 |

i.

Date : Title : Page No.: 26 Perocedure :-) give the connections as per circuit diag with R load with ammeter & voltmeter 2) connect the firing pulses from the firing unit do recepcetine SCR's un pour unit. 3) connect the ilp supply of 30-300 from the centue lapped., TIF & loading enhastait at OP desminal. 4) switch on pourse unit & the firing unit switch on the MCB in power unit & Switch on trigging pulses in fing unit 3) set furguery division to 2. At any firing angle, note waveform accors load vo g note ofp voltage & cuesure ereadings from voltmeter & ammétie



Date : Title : Page No.: 27 -1) Note off vollage waveform for different furguerry division 8) Note ofp vollage & current. a) connect to RE & receptent the above steps. Result: Hence we studied the 1-0 cyclo connectu with R & PL load is verified 612/2/8/2J

Circuit diagram. 17 , 4 × c, C 1 7 L (0.30) RL -1 N (50 A12N) 12 02 A2 - T2 (2 61 Gladd graph (ur) 1 ON No. vac W VO/ $\dot{\mathbf{v}}_{\mathbf{u}}$

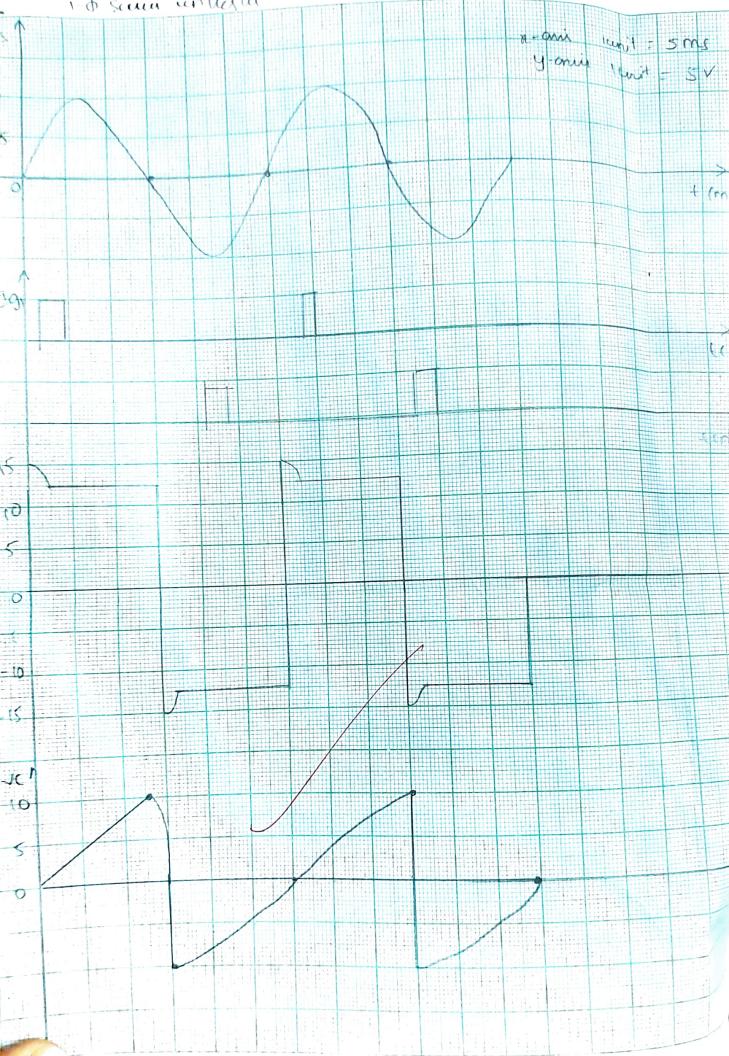
Date : 30-7-21 Title: 8' single phane scenice inverter with Page No.: 20 R and RL loads Aim: 10 constanct single phase scare innerter cucuit & to study its operation with R & RL load. Apparatue:-1) servies inverter cenit. 2) heading Rheastart - 502/24. 3) Regulated pours supply - co-30)~ 4) Inductor - 50 mill 2A. 5) Digital meettimetre. patch caude. 6) shieg: The invertie un which commutating 7) CPO. components are permanently connect in seemis with load called series innerthe series invertre van also darsifieel as self commutated inventures & tood commutated inventures $F = \frac{1}{2(10N + 10FF)} + 2.$

Obseenvations R N= 6.18

| inne Period | Frequency (112) | OLD voltage |
|----------------|--------------------|-------------------|
| sm s | 637 | Guim? |
| Sims | 56-6 | 83.2 m |
| sims | 91.3 | (5. mv 63.1 mv |
| 5 ms | 94.9 | -24.CMr |
| sms | 107-2 | 20.9 |
| 5 m 1 | 129 | -5.25 |
| sms Sms | 151 | 44.4 |

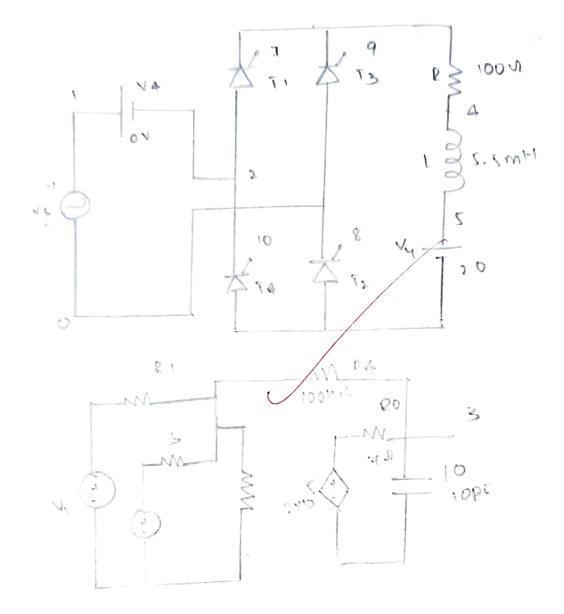
| sime period | E sequency | 0 P V |
|-------------|------------|-----------|
| Cm 2 | 81.4 | 26 mV |
| 7.m7 | 83.4 | . ya. amy |
| Smis | 93.6 | St. Imv |
| Sml | 96.6 | -34.9 m V |
| 2002 | 96.9 | -53.0 mv |
| S m (| 2 6 | - 31.1 |
| (ms | 60 | 37-2 |

| | Date : |
|---|--|
| Title : | Page No. : 29 |
| Perocedure:) Give the connection per circuit with R-toad. a) connect the gale cathode dumin empective pointe on firing unit. 3) Adjust the De supply voltage on De supply & firing unit. | diagnam rale of scristo to zov & switch |
| 4) set funquincy at particular obsume ofp vouveform vo,, vr, on CRO & note vouveform. | position g , $v_{\overline{12}}$, $v_{\overline{11}}$, $v_{\overline{12}}$, $v_{\overline{11}}$ |
| | and noti |
| 6) connect Re bad & note & supeate above steps. | olp voltage |

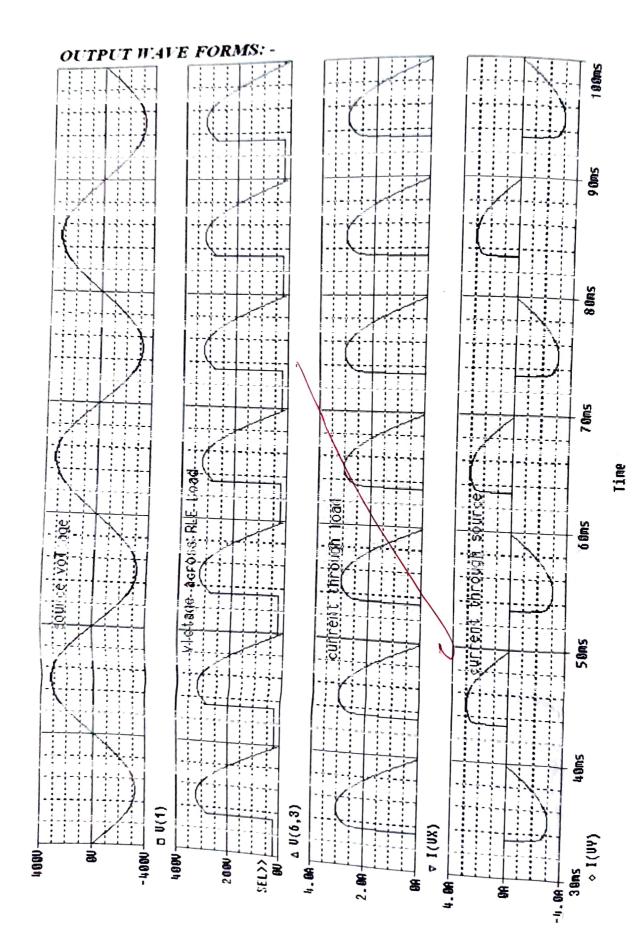


Date : Title : Page No.: 30 Result : Hence obseeved the single phase service unreated with R & RI load. 15 Ryl, 10/21

Count d'agram

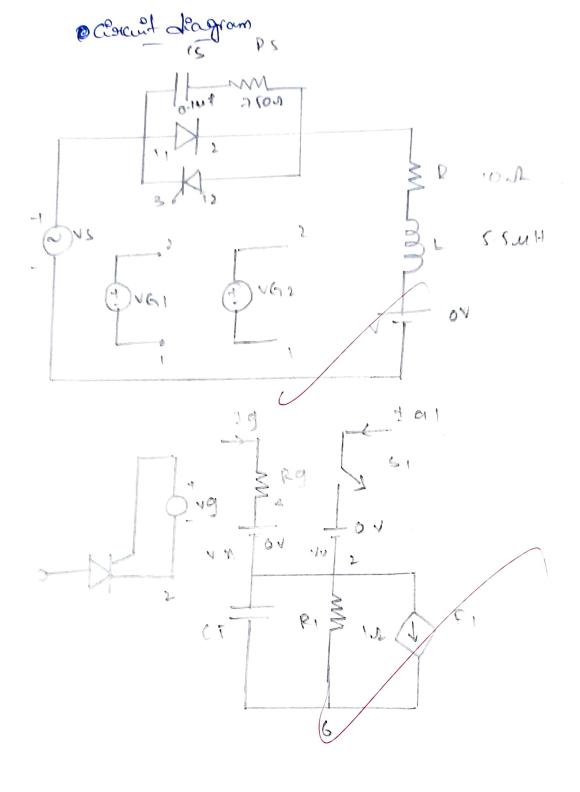


| Title: 9. Single phonse full connecter using Page No.: 31 |
|---|
| RI and E load. |
| |
| Aim: 10 simulate single phan full connectu using |
| pspice . |
| |
| Apparatur: computer |
| pspice software. |
| PSPICE SUPERATION |
| |
| |
| code : |
| |
| VGIG & PULSE COV 10V 3333.3305 INS INS |
| 10005 200005) |
| |
| VG 27 O DULSE CON 10N 3333.3205 INS INS 100 US |
| VG 27 O PULSE COV 10V 33333305 INS INS 100005 2000001) |
| |
| VG 38 2 PULSE CO.10V 13333.3305 INS INS (0005 |
| 2000001) |
| VG 49 1 POLSE CO 100 13333.3304 INS INS 10004 |
| 200002) |
| R2 4 100 OHM |
| LUS S.S MM |
| Vx 53 DC 20V |
| VY 10 IDC LOV |
| |
| |
| |



| Title : Date : |
|---|
| Page No.: 32 |
| x7, 12 67 SCP |
| × 72 3 0 70 SCR |
| X73 0 2 8 2 SCR |
| XTY 3191 SCR |
| · SUBCKI |
| SCP 1232 |
| SI 1562 5MOD |
| RG 3450 |
| NX A 2 DC OV |
| VY S 7 DE OV |
| DT 7 2 DMOD |
| PT 6 2 1 |
| CT 6 2 10 0F F1 2 6 pow(2) 0x Vy 050 11. |
| F_1 2 6 (POW(L) O_{A} (S) |
| • NODEL SHOD USWITCH & RON=0.0105 ROFF = 10 E + 5 VON=0.5V VOFF = 00] |
| • MODEL DMOD D[]= 2.2 E - 15 B V= 1200 V TT= 0 |
| C30:0] |
| . ENDS SCR |

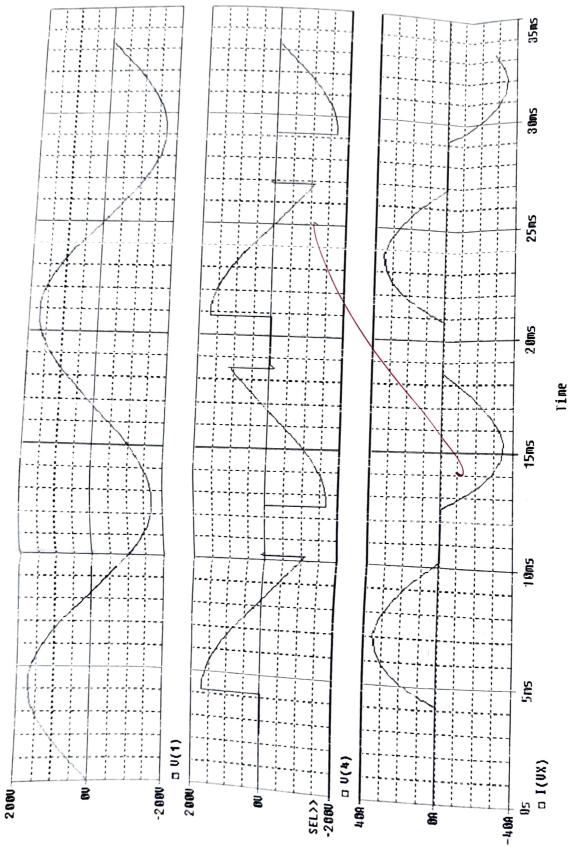
| Title : | Date : Page No. : 33 |
|--|-------------------------|
| - TRAN 5005 100 ms 30 ms | 2042 |
| · OPTIONS ABSTOL = 1.00 N RETOL | = 10N UNTOL =0.01 |
| TTLS = 20000 | |
| · FOUR JOHZ ICUY) | |
| · PROBE | |
| · END · | |
| Result: verified single phan mulog er a e bads Mille Mille A | fully connectu |
| | |
| | |
| | |
| | |
| | |



·

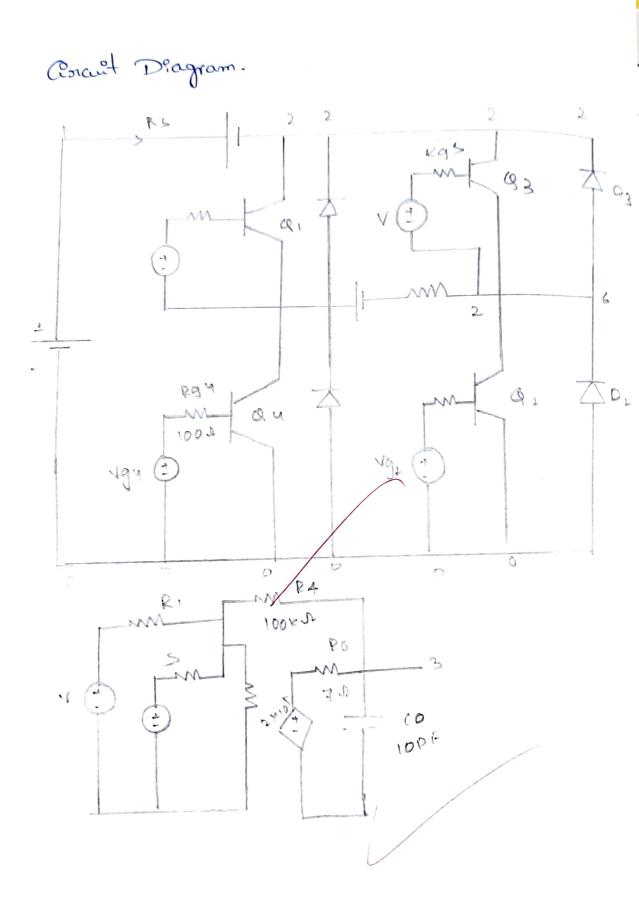
| Title: 10. Single Phase Ac voltage contuctue Date: 30-7-21 using Re Load |
|---|
| the load |
| stimulate gipale also with |
| dim : 20 stimulaile single phase ac voltage |
| controlles using PSPICE. |
| |
| Appasatus :- |
| computu |
| pspice software. |
| |
| Peroguain :- |
| VS LO SIN CO 1900 BOHZ) |
| VGI 2 4 PULSE COU LOU 4166.705 INS INS |
| 10005 16666.705) |
| VG2 3 1 PULSE [00 100 1250005 INC INS 10005 |
| 16666.705) |
| R 4 5 2.5 |
| L 5 6 6 5 m H |
| VX 6 O °C OV |
| (S 1 7 0.0F |
| R3 7 4 750 |
| X7, 1 4 2 4 SCR |
| |

OUTPUT WAVE FORMS: -

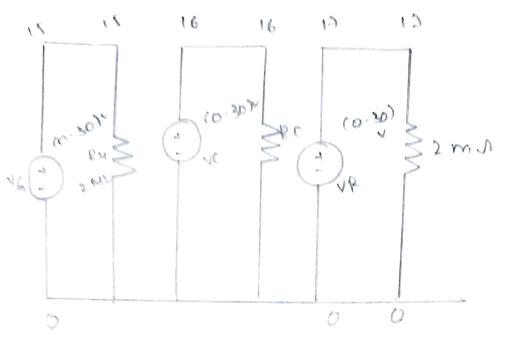


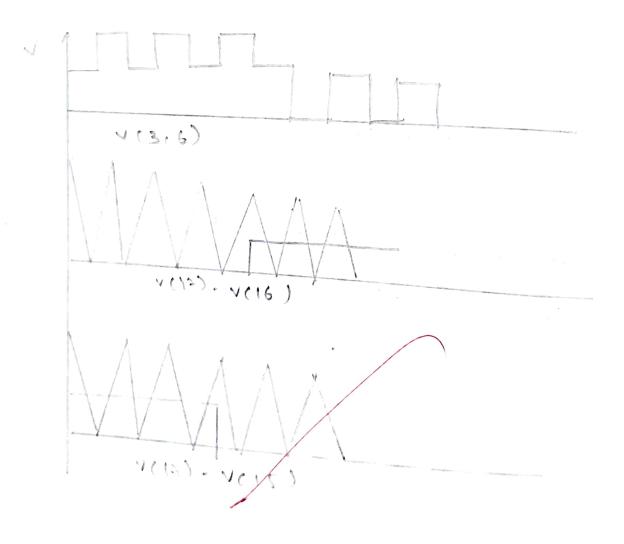
Date : Page No. : 35 Title : I SCR. 3 1 xT2 4 SCR 3 2 1 2 SUB CKT 5 6 2 SMOD 1 SI 50 A 3 RG 2 DC IOV 4 VX 2 00 01 5 NY 6 1 2 RT 2 10 UP 6 pocy12) vy vy oso II 6 CT · MODEL SMOD USWITCH (RON=0.0) ROFF=10H3 VON=0-1 21 2 · ENDS SCR TRAN 1005 33:33 ms · OPTIONS ABSTOL = 1.000 RETTOL = 1000 UNTOL = 1000 · FOUR GOTT2 AY · END ·

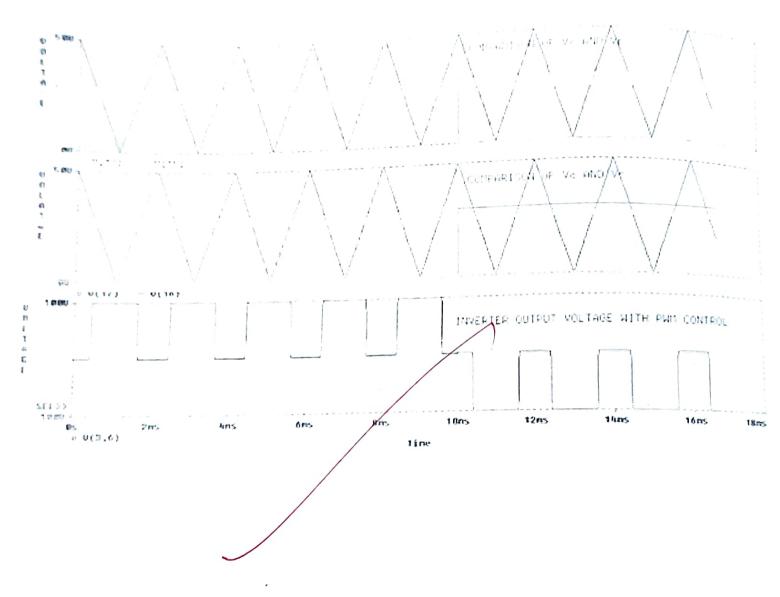
Date : Title : Page No. : 36 Result : Hence verified to voltage contubled using Ri load. BRy 1 2/2/21



| Title: Single phase promisinger Date: 30-7-21 Page No: 20 |
|---|
| Aim: Jo stimulate single phase prom vinnester using PSPICE. |
| Apprualue: computer and pspice software |
| Peroguam:- Vs 1 0 DC 100 V |
| VR 17 O POLSE (SON ON O IMS IMS INS 2MS) |
| RE 17 O 2MEG VCI 15 O PULSE CO-30 V O IMS INS IOMS 20MS) RCI 15 O 2MEG. |
| VC3 16 0 POLSE (0-30 VIOMS INS INS IOMS 20MS |
| $\begin{array}{cccccccccccccccccccccccccccccccccccc$ |
| V_{y} 1 2 DC OV D1 B 2 DMOD D DMOD |
| $ \begin{array}{cccccccccccccccccccccccccccccccccccc$ |







| Date : Page No.: $3r$ NODE1 DNOD D(15=3)2E - 155 $8v = 1690v$) a1 2 =13 $9, MOD$ a1 3 13 0 $9, MOD$ a1 3 13 0 $9, MOD$ a13 0 $9, MOD$ $0.5 = 6.435F$ $BF = u164v$ $c1c = 3.647P$ a13 0 $0.9, MOD$ $0.5 = 6.435F$ $BF = u164v$ $c1c = 3.647P$ a14 0 0.000 0.0000 0.0000 0.0000 0.0000 a15 13 10000 0.0000 0.0000 0.00000 0.00000 a15 12 11 10000 0.00000 0.000000 0.000000 a16 12 3 3.0000000000000 $0.00000000000000000000000000000000000$ | | |
|--|---|--------------------------------------|
| . NODEL DNOD D($15 = 3 \cdot 2e - 1/5$ $Bv = 1690V$) a_1 2 = 3 a_1 mod a_2 2 = 3 a_2 mod a_3 2 = 11 e_2 $Bvod$ a_4 3 = 13 O a_1 mod a_4 3 = 13 O a_2 mod a_5 2 = $u - 493P$) Rai 8 $= 1600$ OHM Rai 12 11 100 OHM Rai 13 12 10 00 OHM Rai 14 15 $= 8 - 3200M$ Ypw_2 14 15 10 O OHM Ypw_3 14 16 12 $= 900M$ Xpw_4 13 16 10 O PWM Xpw_4 13 16 10 O PWM P_2 3 $= 11k$ P_1 1 $= 11k$ P_2 3 $= 11k$ P_3 3 $= 11k$ P_4 3 $= 11k$ P_5 $= 3 = 100K$ | Title : | |
| a_1 c q q mod a_2 a_3 a_1 c q mod a_4 3 13 d mod a_4 a_4 a_6 a_6 a_7 a_5 a_6 a_7 a_7 a_7 a_6 a_7 a_7 a_7 a_7 a_6 a_7 a_7 a_7 a_7 a_6 a_7 a | NODEL DNOD DC 15= 3-2E - 1.5 | |
| RG1 10 9 100 0HM RG3 12 11 100 0HM RG4 14 13 100 0HM RG4 14 13 100 0HM RG4 14 13 100 0HM RG4 14 15 8 3PWM YPW2 14 15 10 0PWM YPW3 14 16 12 6 PWM XPW4 13 16 12 3 YPW4 14 16 12 3 4 R1 1 5 1K 12 3 4 R1 1 5 1K 15 1K 15 R1 1 5 1K 12 3 4 R1 1 5 1K 12 3 4 R1 1 5 1K 14 15 16 R2 2 5 1K 12 14 16 12 14 | $\begin{array}{cccccccccccccccccccccccccccccccccccc$ | BE= U164 CIC= 3.68FP CJE= U-493P) |
| $\begin{array}{cccccccccccccccccccccccccccccccccccc$ | RG1 10 9 100 0HM RG2 12 11 100 0HM RG3 12 11 100 0HM RG4 14 13 100 0HM RG4 14 13 100 0HM XPW1 14 15 8 3PWM YPW2 14 15 10 0PWM YPW3 14 16 12 6 PWM | |
| EI 6 4 0 5 2E+J | $\begin{array}{cccccccccccccccccccccccccccccccccccc$ | 5 |

| Title : | Date: Page No.: ₃₉ |
|---|----------------------------------|
| | 1 ago 110. 29 |
| ends prom | |
| - TRAN 1005 16.67 NS 0 1005 | |
| · probt | |
| · OPTIONS ABSTOL = 1.0000 RELTOL | =0.01 UNTOL =0.) |
| ITLS = 20000 | |
| • END | |
| • END Result: Vesified the working 1- & PWM unvastu using pspic Mil 218/21 | 8 operation of e. |
| -DUSTING | |
| | |
| | |
| | |
| | |
| | |
| | |